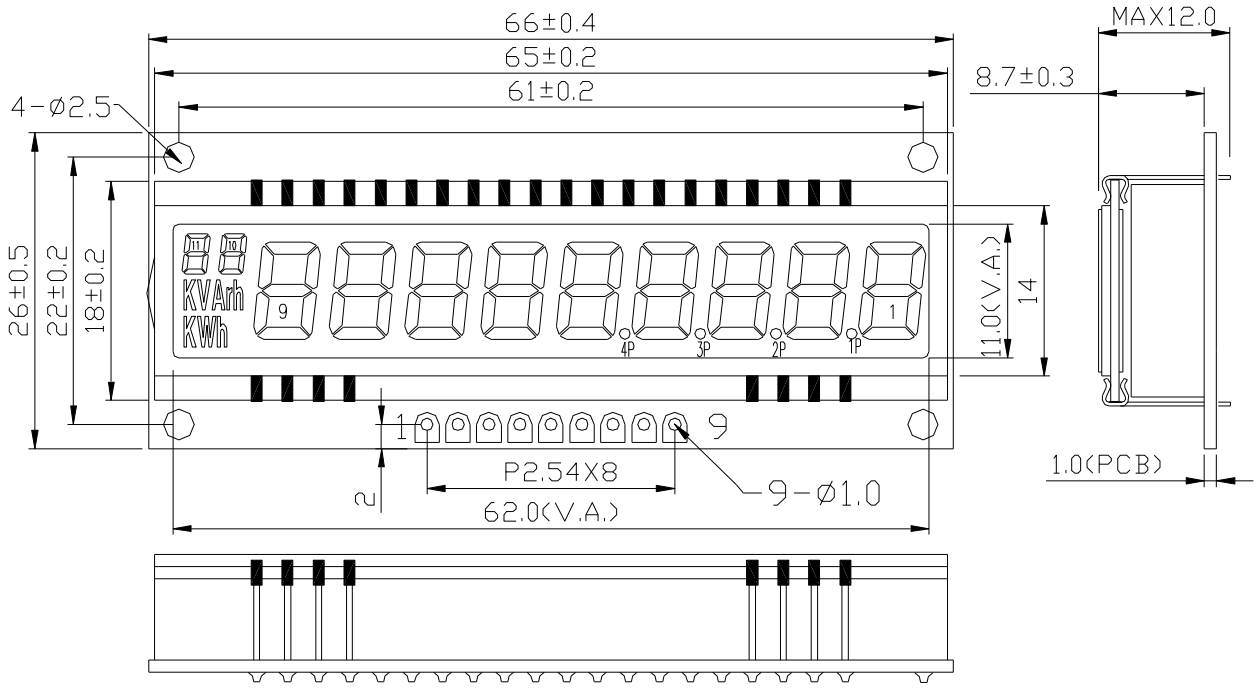
XIAMEN OCULAR

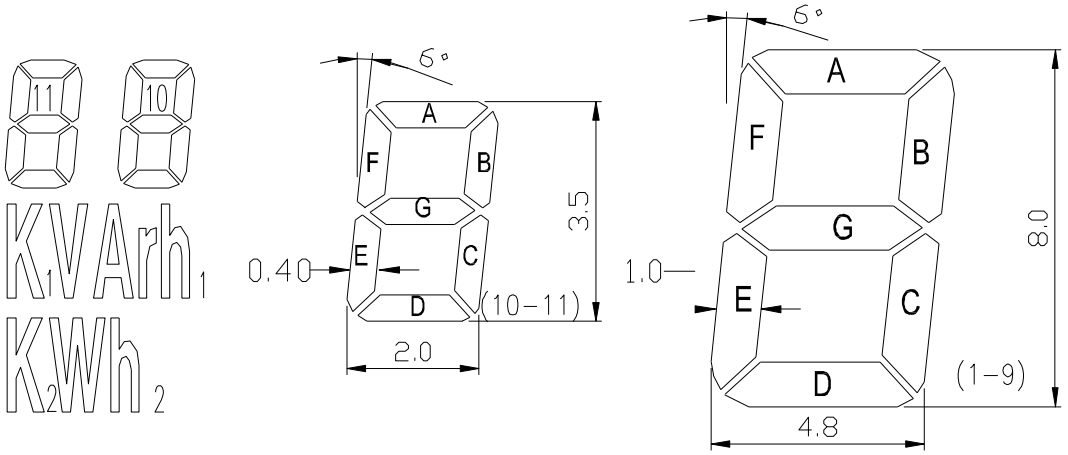
GDM076-FL-YBW/3.6V SPECIFICATIONS OF LCD MODULE

CONTENTS

1. Mechanical diagram



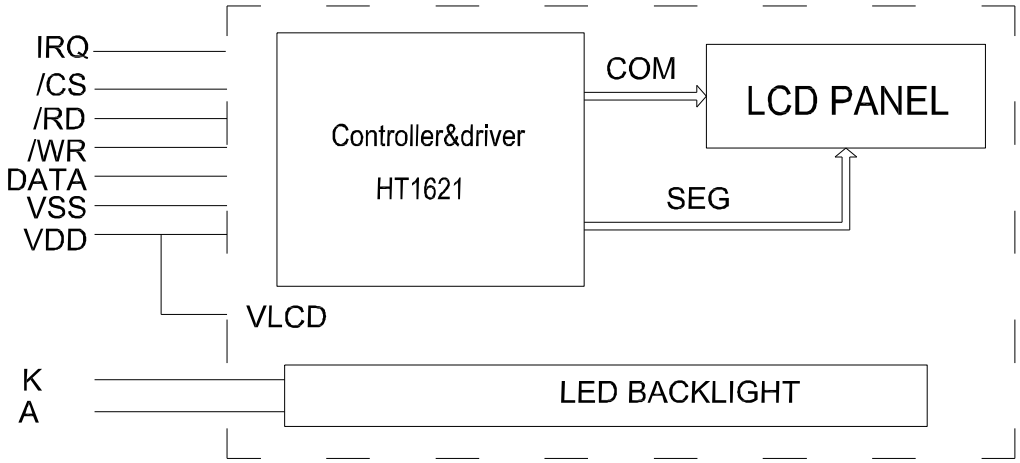
RAM Mapping



ADDR.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
D3	K1	V	11A	11B	10A	10B	9A	9B	8A	8B	7A	7B	6A	6B	5A	5B	4A	4B	3A	3B	2A	2B	1A	1B
D2	h1	K2	11F	11G	10F	10G	9F	9G	8F	8G	7F	7G	6F	6G	5F	5G	4F	4G	3F	3G	2F	2G	1F	1G
D1	A	r	11E	11C	10E	10C	9E	9C	8E	8C	7E	7C	6E	6C	5E	5C	4E	4C	3E	3C	2E	2C	1E	1C
D0	W	h2	11D	--	10D	--	9D	--	8D	--	7D	--	6D	--	5D	--	4D	4P	3D	3P	2D	2P	1D	1P

Display Mode: STN (Yellow-green), Positive / Transflective
Driving method: 1/4duty 1/3bias
Viewing angle: 6:00 O'CLOCK

2. Block diagram



*** Notes:**

The voltage applied to VLCD pin must be lower than VDD.
Adjust VR to fit LCD display, at V_{DD} =3.6V, V_{LCD} =3.6V,
Adjust R (external pull-high resistance) to fit user s time base clock.

3. Absolute Maximum Ratings

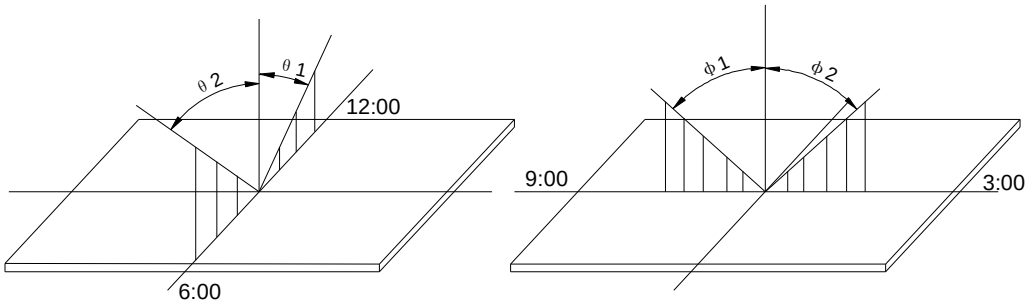
Item	Symbol	Min	Max	Unit
Power Voltage	V_{DD} -V_{SS}	0	5.5	V
Input Voltage	V_I	V_{SS}	V_{DD}	
Operating Temperature Range	V_{OP}	-20	+75	℃
Storage Temperature Range	T_{ST}	-30	+85	

4.Description Of Terminals

Pin No.	Pin Name	Input/ Output	External Connection	Function
1	/CS	Input	MPU	Chip selection input with pull-high resistor When the CS is logic high, the data and command read from or written to the HT1621 are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the HT1621 are all enabled.
2	/RD	Input	MPU	READ clock input with pull-high resistor Data in the RAM of the HT1621 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	/WR	Input	MPU	WRITE clock input with pull-high resistor Data on the DATA line are latched into the HT1621 on the rising edge of the WR signal.

4	DATA	—	MPU	Serial data input/output with pull-high resistor
5	VSS	—	Power Supply	VSS: GND
6	VDD	—		VDD: +3.6V
7	/IRQ	Output		Time base or WDT overflow flag, NMOS open drain output
8	K			Power for Backlight (+0v)
9	A			Power for Backlight (+4.0v)

5. Optical Characteristics

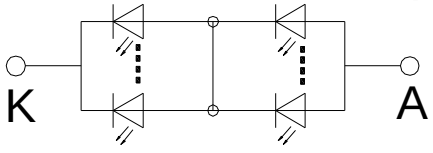


STN type display module (Ta=25℃, VDD=3.6V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ 1	$C_r \geqslant 3$		20		deg
	θ 2			40		
	Φ 1			35		
	Φ 2			35		
Contrast ratio	C_r		-	10	-	-
Response time (rise)	T_r	-	-	200	250	ms
Response time (fall)	T_r	-	-	300	350	

6. Electrical Characteristics

Ø Backlight circuit diagram(COLOR: Yellow-Green) light: 9x2=18



Ø LED ratings (voltage= 4.0V)

Item	Symbol	Min	Typ.	Max	Unit
Forward Voltage	V_F	3.8	4.0	4.2	V
Forward current	IF		90	100	mA
Power	P			500	mW
Peak wave length	λp		568		nm
Luminance	Lv		200		Cd/m^2

Ø DC Characteristics

Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_O$	T_A=25℃	—	3.6	—	V
Input voltage	V_{DD}		3.4	3.6	3.8	V
Supply current	I_{DD}	V_{DD}=3.6V;T_A=25℃	—	0.2	0.5	mA
Input leakage current	I_{LKG}		—	—	1.0	μA
“H” level input voltage	V_{IH}		2.2	—	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	—	0.6	V
“H” level output voltage	V_{OH}	L_{OH}= -0.25mA	2.4	—	—	V
“L” level output voltage	V_{OL}	L_{OL}=1.6mA	—	—	—	V
Backlight supply voltage	V_F		—	4.0	—	V

Ø AC. Characteristics

VDD=3.6V, Ta=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SYS1}	System clock	On-chip RC oscillator	—	256	—	KHZ
f_{SYS2}	System clock	Crystal oscillator	—	32.768	—	
f_{LCD}	LCD clock	On-chip RC oscillator	—	$f_{SYS1/1024}$	—	HZ
		Crystal oscillator	—	$f_{SYS2/128}$	—	
t_{COM}	LCD Common Period	N: Number of COM	—	n/f_{LCD}	—	S
f_{CLK1}	Serial Data Clock (WR pin)	Duty cycle 50%	—	—	150	KHZ
f_{CLK2}	Serial Data Clock (RD pin)	Duty cycle 50%	—	—	75	
f_{TONE}	Tone Frequency	On-chip RC oscillator	—	2 or 4	—	
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	/CS	—	250	—	ns
t_{CLK}	WR, RD Input Pulse Width (Figure 1)	Write mode	3.34	—	—	us
		Read mode	6.67	—	—	
t r ,t f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	120	—	ns
t su	Setup Time for DATA to WR, RD Clock Width (Figure 2)	—	—	120	—	
t h	Hold Time for DATA to WR, RD Clock Width (Figure 2)	—	—	120	—	
t su1	Setup Time for CS to WR, RD Clock Width (Figure 3)	—	—	100	—	
t h1	Hold Time for CS to WR, RD Clock Width (Figure 3)	—	—	100	—	

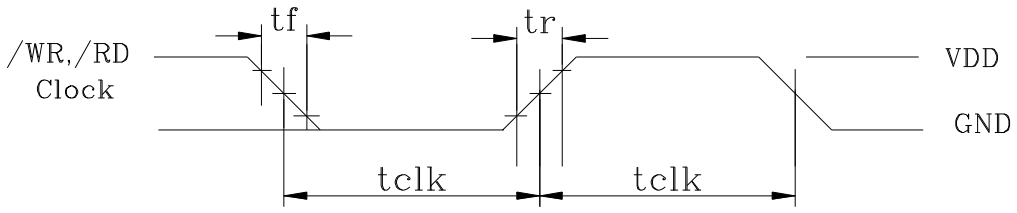


Figure 1

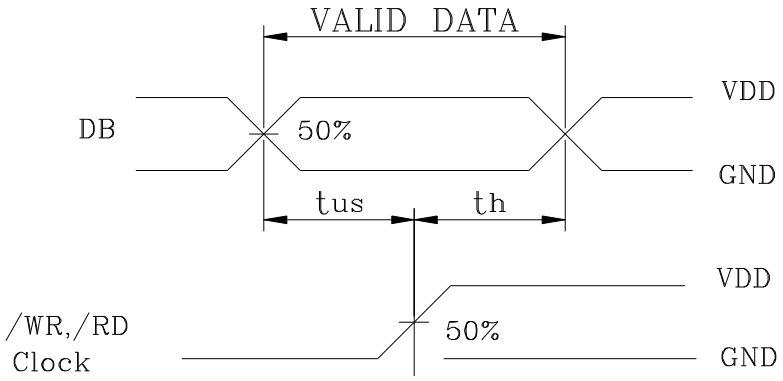


Figure 2

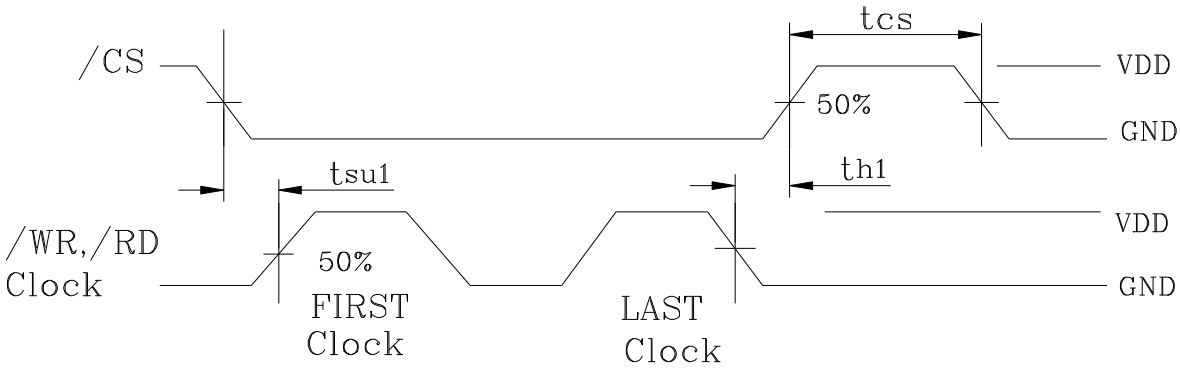
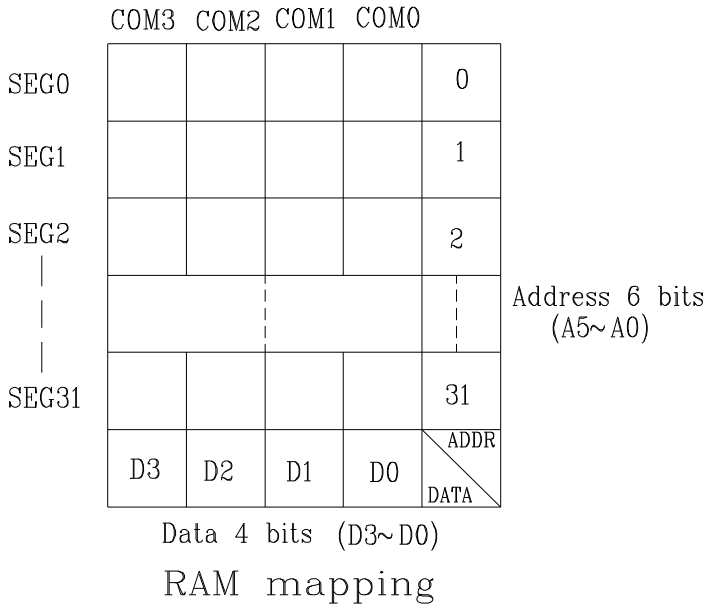


Figure 3

8. Functional Description

Display memory-RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



RAM mapping

System oscillator

The HT1621 system clock is used to generate the time base/watchdog timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the HT1621 is at the SYS DIS state.

Name	Command Code	Function
LCD OFF	**1 0** 00 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	**1 0** 00 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	**1 0** 00 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

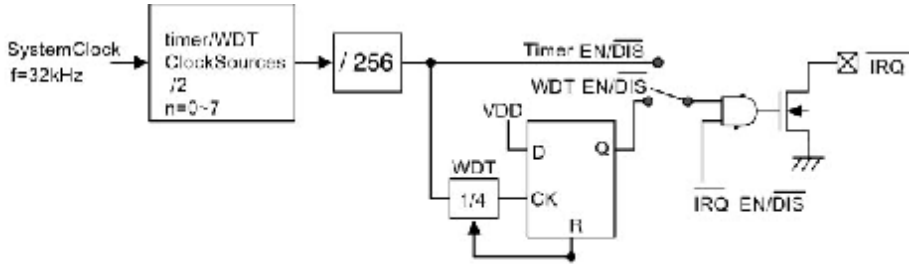
Time base and watchdog timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watchdog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other

sub-systems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the IRQ out-put by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$F_{WDT} = \frac{32kHZ}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz. If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the IRQ pin). After the TIMER EN command is ransferred, the WDT is disconnected from the IRQ pin, and the output of the time base generator is connected to the IRQ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command re-spectively. Before executing the IRQ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the IRQ pin will stay at a logic low level until the CLR WDT or the IRQ DIS command is issued. After the IRQ output is disabled the IRQ pin will remain at the floating state. The IRQ output can be enabled or disabled by executing the IRQ EN or the IRQ DIS command, respectively. The IRQ EN makes the output of the time base generator or of the WDT time-out flag appear on the IRQ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions. On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the HT1621 will continue working until system power fails or the external clock source is removed. After the system power on, the IRQ will be disabled.



Timer and WDT configurations

LCD driver

The HT1621 is a 128 (32x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table. The bold form of **1 0 0**,namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands; the HT1621 can be compatible with most types of LCD panels.

Command format

The HT1621 can be configured by the S/W set-ting. There are two mode commands to configure the HT1621 resources and to transfer the LCD display data. The configuration mode of the HT1621 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

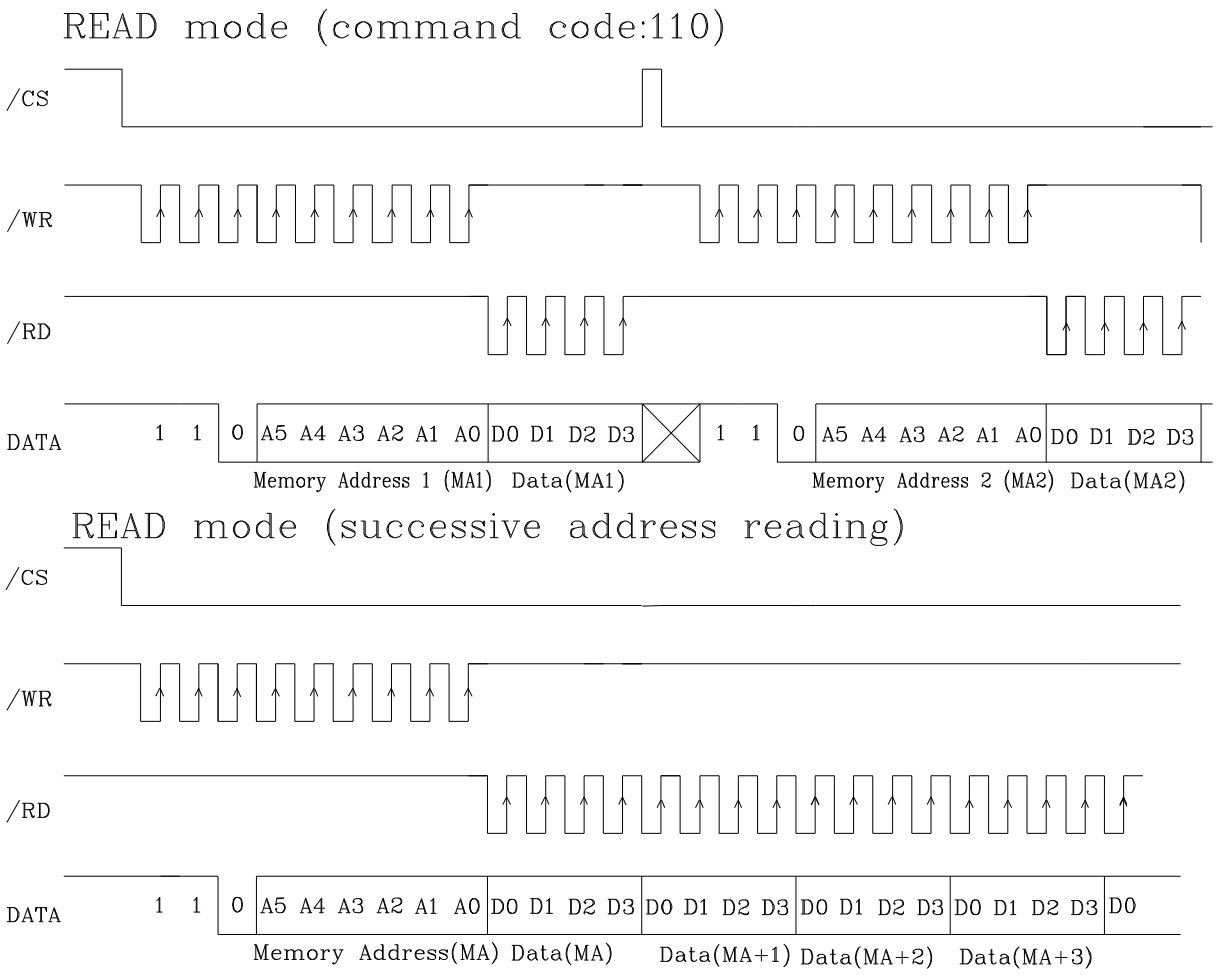
Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS pin should be set to "**1**" and the previous operation mode will be reset also. Once the CS pin returns to "**0**" a new operation mode ID should be issued first.

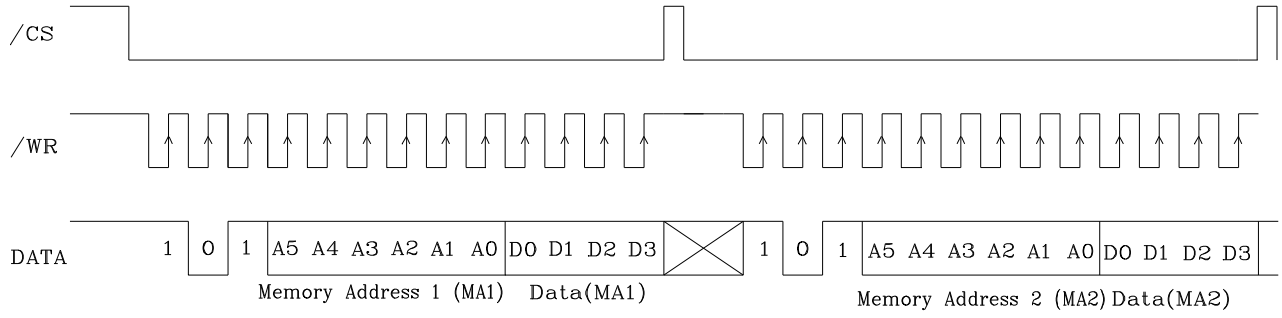
Interfacing

Only four lines are required to interface with the HT1621. The CS line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1621. If the CS pin is set to **1**, the data and command issued between the host controller and the HT1621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the RD signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the RD signal. The WR line is the WRITE clock input. The data, address, and command on the DATA line are all clock-ed into the HT1621 on the rising edge of the WR signal. There is an optional IRQ line to be used as an interface between the host controller and the HT1621. The IRQ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the IRQ pin of the HT1621.

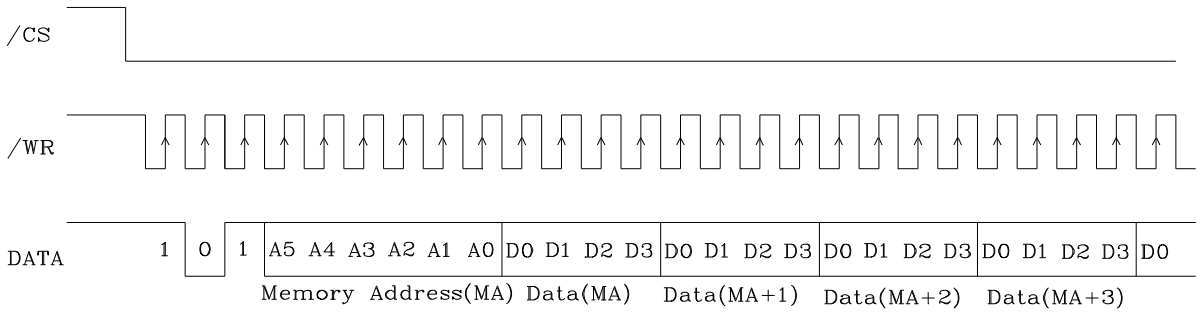
9. Timing Diagrams



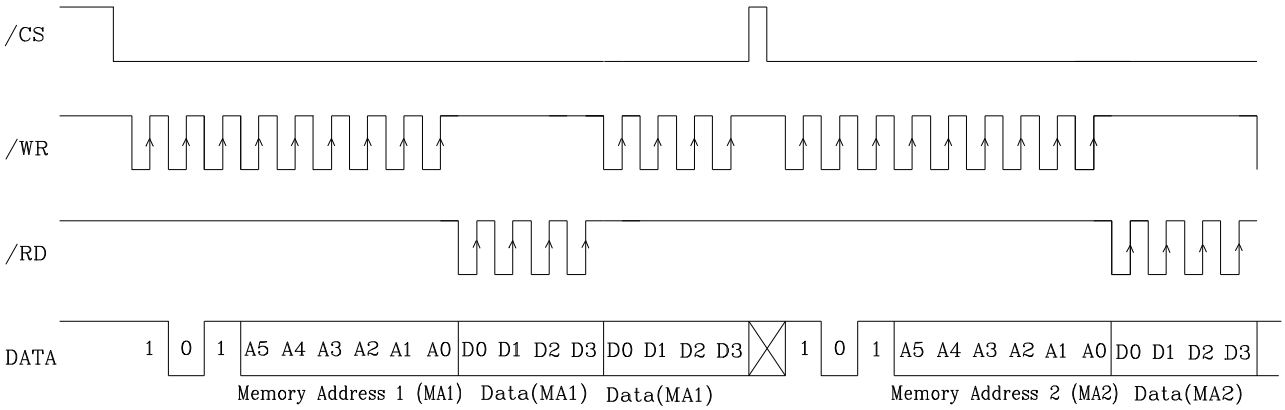
Write mode (command code 101)



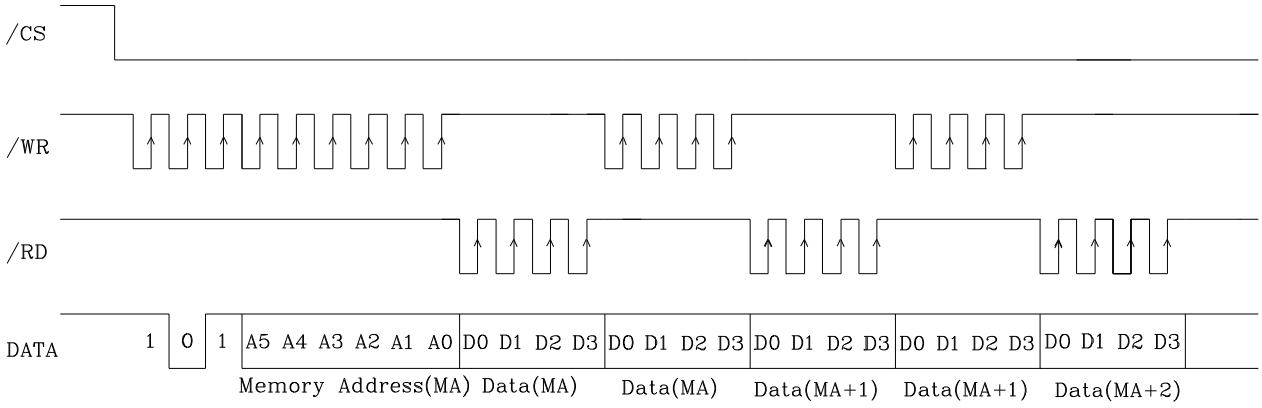
Write mode (successive address writing)

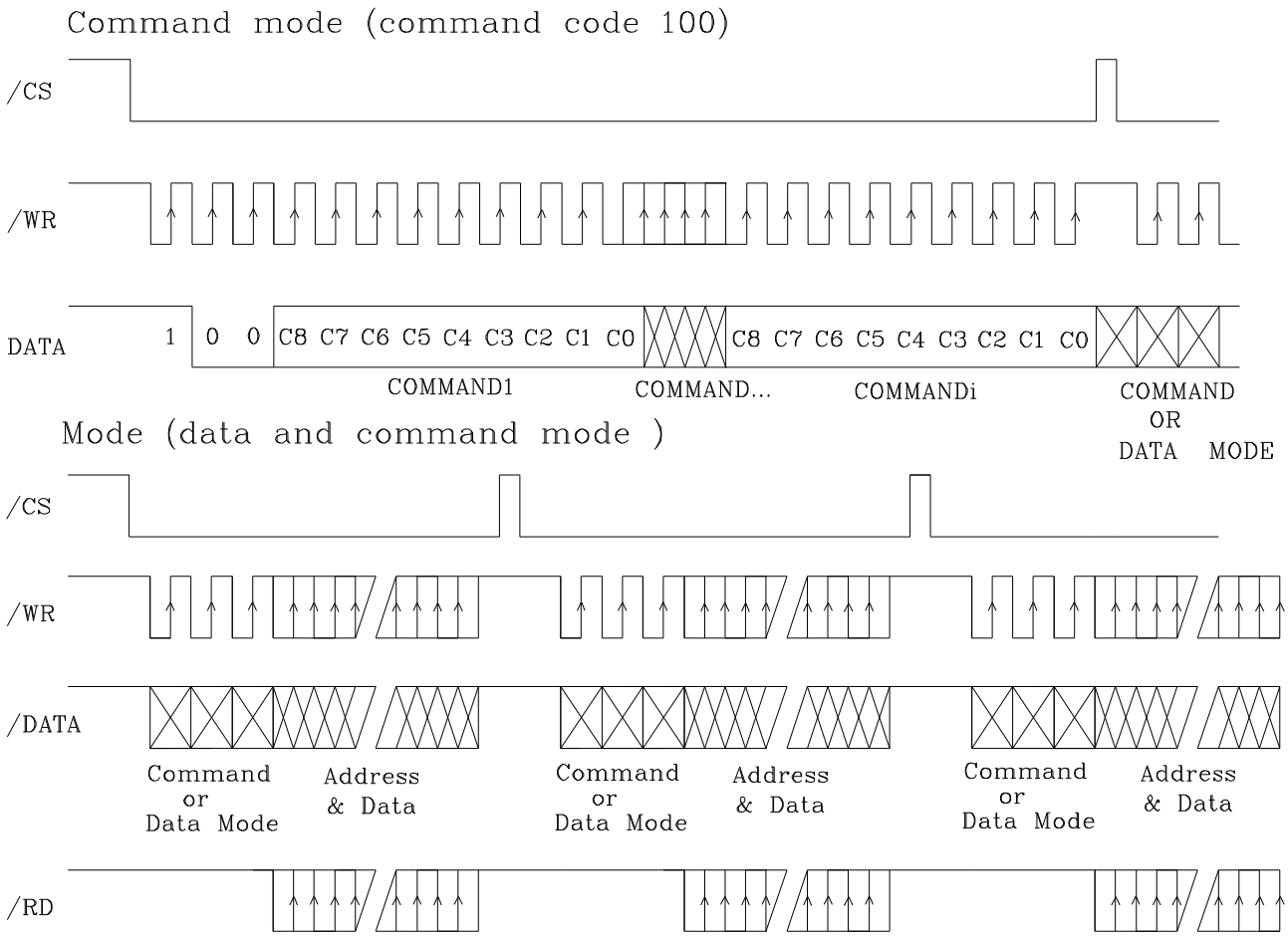


Read-Modify-Write mode (command code 101)



Read-Modify-Write mode (successive address accessing)





Note:

It is recommended that the host controller should read in the data from the DATA line between the rising edge of the RD line and the falling edge of the next RD line.

10. Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	**1 1 0**	A5A4A3A2A1A0 D0D1D2D3	D	Read data from the RAM	
WRITE	**1 0 1**	A5A4A3A2A1A0 D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**1 0 1**	A5A4A3A2A1A0 D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	**1 0 0**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	**1 0 0**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**1 0 0**	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	**1 0 0**	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	**1 0 0**	0000-0100-X	C	Disable time base output	
WDT DIS	**1 0 0**	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	**1 0 0**	0000-0110-X	C	Enable time base output	
WDT EN	**1 0 0**	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	**1 0 0**	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	**1 0 0**	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	**1 0 0**	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	**1 0 0**	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	**1 0 0**	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	**1 0 0**	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	**1 0 0**	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	**1 0 0**	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	**1 0 0**	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	**1 0 0**	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	**1 0 0**	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	**1 0 0**	100X-0XXX-X	C	Disable IRQ output	Yes

Name	ID	Command Code	D/C	Function	Def.
IRQ EN	**100**	100X-1XXX-X	C	Enable IRQ output	
F1	**100**	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	**100**	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	**100**	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	**100**	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2 s	
F16	**100**	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4 s	
F32	**100**	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8 s	
F64	**100**	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16 s	
F128	**100**	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32 s	Yes
TEST	**100**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**100**	1110-0011-X	C	Normal mode	Yes

Notes:

X : Don't care

A5~A0 : RAM addresses

D3~D0 : RAM data

D/C : Data/command mode

Def. : Power on reset default

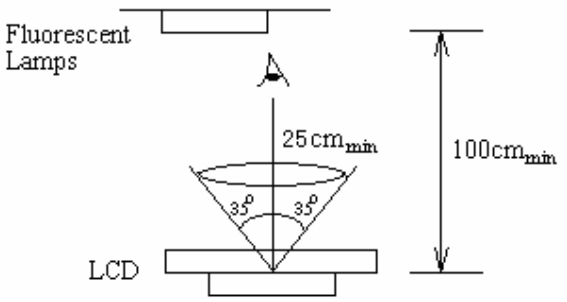
All the bold forms, namely**110**, **101**, and **100**, are mode commands. Of these, **100** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1621 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1621.

QUALITY SPECIFICATIONS

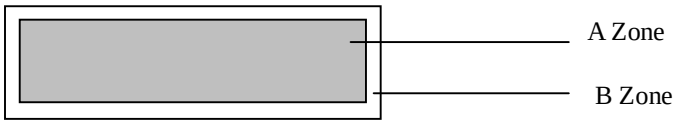
Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 25 cm or more.

Viewing direction for inspection is 35° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).
B Zone: Non-active display area (outside viewing area).

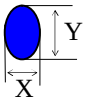
Specification of quality assurance

AQL inspection standard
Sampling method: GB2828-87, Level II, single sampling
Defect classification **(Note: * is not including)**

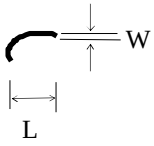
Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
		Wrong or missing component	11	
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

Note on defect classification

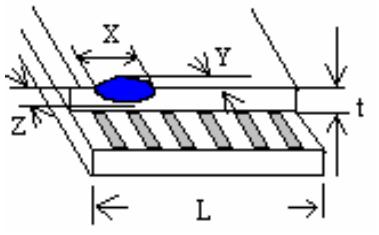
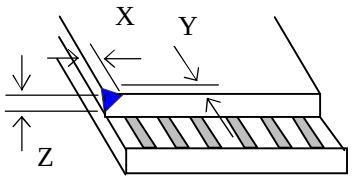
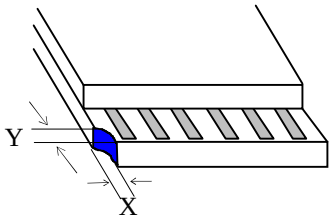
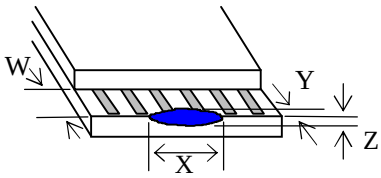
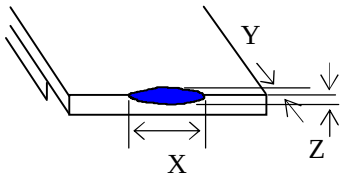
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td></td><td>LC leakage</td></tr>
<tr><td></td><td>Flickering</td></tr>
<tr><td></td><td>No display</td></tr>
<tr><td></td><td>Wrong viewing direction</td></tr>
<tr><td></td><td>Wrong Back-light</td></tr>
<tr><td>2</td><td>Contrast defect</td><td rowspan="2">Refer to approval sample</td></tr>
<tr><td></td><td>Backgroundcolor deviation</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

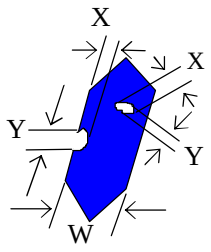
$\phi = (X+Y)/2$</td><td> 

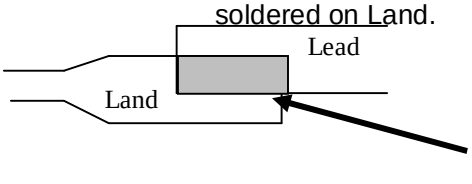
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>$\phi \leq 0.10$</td><td>Disregard</td></tr>
<tr><td>$0.10 < \phi \leq 0.15$</td><td>2</td></tr>
<tr><td>$0.15 < \phi \leq 0.25$</td><td>1</td></tr>
<tr><td>$\phi > 0.25$</td><td>0</td></tr>
</table>
Unit：Inch^2</td></tr>
<tr><td>4</td><td>Line defect,

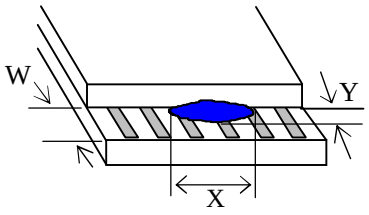
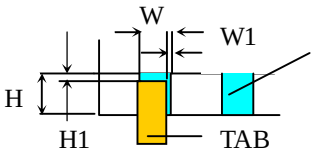
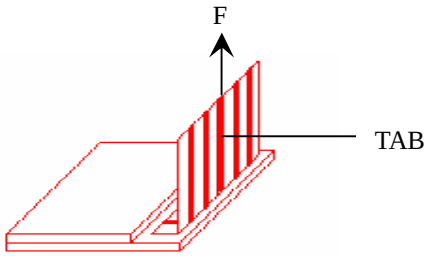
Scratch</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.05>W</td><td rowspan="3">Disregard</td></tr>
<tr><td>3.0>L</td><td>0.1>W>0.05</td></tr>
<tr><td>2.0>L</td><td>0.15≥W>0.1</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

No	Item	Criterion
6	Chip Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width L:Glass length	 Acceptable criterion X: < L /8; Y: 0.5mm; Z: ≤t/2  Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t  Acceptable criterion X: ≤3; Y: ≤2; Z: ≤t shall not reach to ITO  Acceptable criterion X: Disregard; Y: ≤0.2; Z: ≤t  Acceptable criterion X: ≤5; Y: ≤2; Z: ≤t/3

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>7</td><td>Segment pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>8</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>9</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>10</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>11*</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

No	Item	Criterion
12	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
13	TAB	1. Position  W1≤1/3W H1≤1/3H 2 TAB bonding strength test  P (=F/TAB bonding width) ≥650gf/cm ,(speed rate: 1mm/min) 5pcs per SOA (shipment)
14	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.

Reliability of LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	48	No abnormalities in functions and appearance
High temp. Operating	70°C	48	
Low temp. Storage	-30°C	48	
Low temp. Operating	-20°C	48	
Humidity	40°C/ 90%RH	48	
Temp. Cycle	0°C ← 25°C →50°C (30 min ← 5 min → 30min)	10cycles	

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (20±8°C), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

Precaution for using LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol, ethyl alcohol or trichlorotriflorothane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting XIAMEM OCULAR
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause

disconnection or defective insulation of terminals.

4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature: 280°C±10°C
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over 40°C is required, the relative humidity should be kept below 60%, and avoid direct sunlight.

Limited Warranty

XIAMEM OCULAR LCDs and modules are not consumer products, but may be incorporated by XIAMEM OCULAR 's customers into consumer products or components thereof, XIAMEM OCULAR does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of XIAMEM OCULAR is limited to repair or replacement on the terms set forth below. XIAMEM OCULAR will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between XIAMEM OCULAR and the customer, XIAMEM OCULAR will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with XIAMEM OCULAR general LCD inspection standard . (Copies available on request)
2. No warranty can be granted if any of the precautions state in handling liquid crystal display above has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.
3. In returning the LCD/LCM, they must be properly packaged; there should be detailed description of the failures or defect.