SPECIFICATION

128*64 Dot Matrix LCD Module

GDSC12864WM-39

(COG)

XIAMEN OCULAR LCD DEVIDES CO.,LTD.

GENERAL SPECIFICATION

Interace With Parallel/Serial MPU

Driving IC:ST7565R

Display Specification

Display Dot Matrix :128*64

Viewing Angle :6:00 Clock

Display Duty:1/65 Driving bias:1/9 Driving voltage:9.0V

Mechanical Characteristics(Unit:mm)

Extenal Dimension:59.8*44.2*5.7

View Area:54.6*32.0

Dots Size:0.36*0.40

Dots Pitch:0.39*0.43

Backlight Specification

1.FORWARD VOLTAGE(Vf):DC 3.1V

2.FORWARD CURRENT(If):90 mA

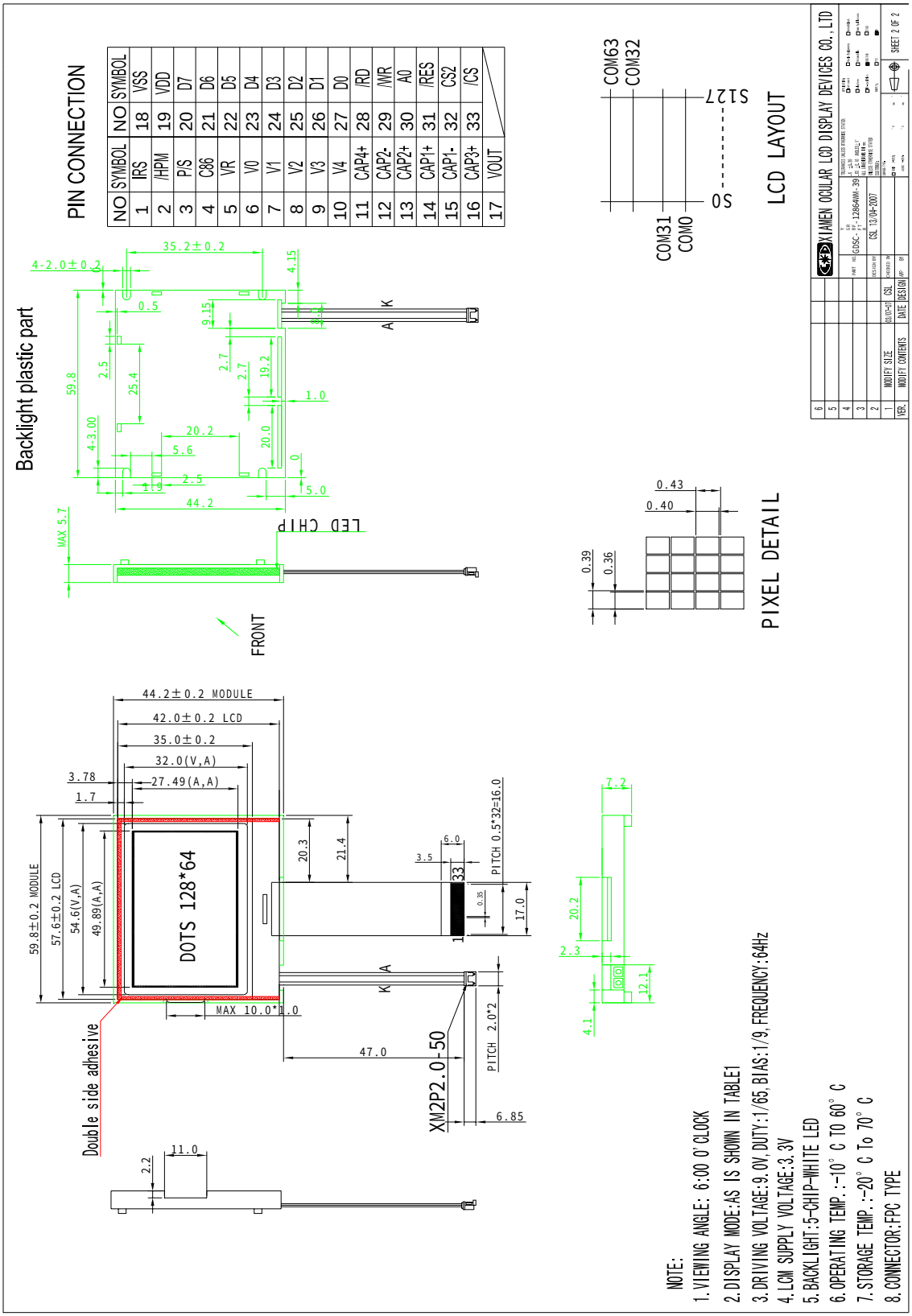
3.LED SITE:SIDE(6 CHIPS)

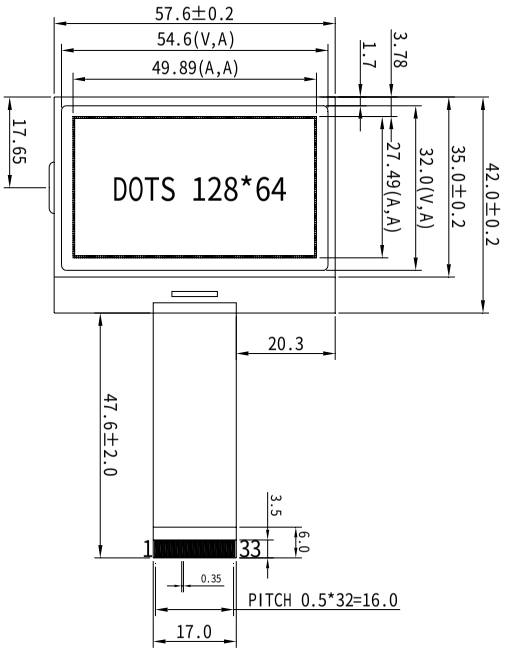
4.OPERATING TEMP.:-20℃ TO 70℃

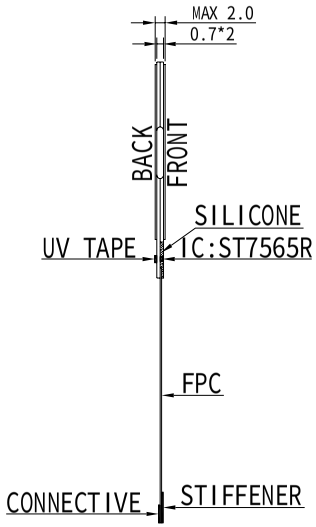
5.STORAGE TEMP.:-30℃ To 75℃

6.LED COLOR:WHITE

External Dimension





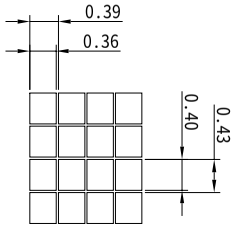


PIN CONNECTION

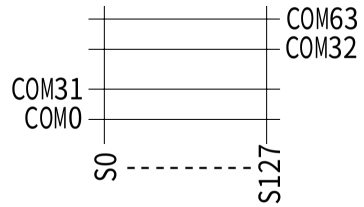
NO	SYMBOL	NO	SYMBOL
1	IRS	18	VSS
2	/HPM	19	VDD
3	P/S	20	D7
4	C86	21	D6
5	VR	22	D5
6	V0	23	D4
7	V1	24	D3
8	V2	25	D2
9	V3	26	D1
10	V4	27	D0
11	CAP4+	28	/RD
12	CAP2-	29	/WR
13	CAP2+	30	A0
14	CAP1+	31	/RES
15	CAP1-	32	CS2
16	CAP3+	33	/CS
17	VOUT		

TABLE1

MODE	R	F	T
Y	POSITIVE,REFLECTIVE YELLOW-GREEN,STN TYPE	POSITIVE,TRANSFLECTIVE YELLOW-GREEN,STN TYPE	POSITIVE,TRANSMISSTIVE YELLOW-GREEN,STN TYPE
G	POSITIVE,REFLECTIVE GRAY,STN TYPE	POSITIVE,TRANSFLECTIVE GRAY,STN TYPE	POSITIVE,TRANSMISSTIVE GRAY,STN TYPE
B		NEGATIVE,TRANSFLECTIVE BLUE,STN TYPE	NEGATIVE,TRANSMISSTIVE BLUE,STN TYPE
F	POSITIVE,REFLECTIVE FSTN TYPE	POSITIVE,TRANSFLECTIVE FSTN TYPE	POSITIVE,TRANSMISSTIVE FSTN TYPE
W		NEGATIVE TRANSFLECTIVE BLACK-WHITE STN	NEGATIVE TRANSMISSIVE BLACK-WHITE STN



PIXEL DETAIL



LCD LAYOUT

NOTE:

1. VIEWING ANGLE: 6:00 O'CLOCK
2. DISPLAY MODE:AS IS SHOWN IN TABLE1
3. DRIVING VOLTAGE:9.0V,DUTY:1/65,BIAS:1/9,FREQUENCY:64Hz
4. LCM SUPPLY VOLTAGE:3.3V
5. OPERATING TEMP.:-10° C TO 60° C
6. STORAGE TEMP.:-20° C To 70° C
7. CONNECTOR:FPC TYPE

VER.	MODIFY CONTENTS	DATE	DESIGN
6			
5			
4			
3			
2			
1			

XIAMEN OCULAR LCD DISPLAY DEVICES CO.,LTD

PART NO. GDSC-YGRBFFT-12864WM-39

DESIGN BY CSL 13/04-2007

CHECKED BY

APP BY

TOLERANCES UNLESS OTHERWISE STATED:
X ±0.30
XY ±0.10 ANGLE±1°
ALL THICKNESS IN mm
UNLESS OTHERWISE STATED

CUSTOMER:

SHEET 1 OF 2

Absolute Maximun Ratings

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		VDD	0.3 ~ 5.0	V
Power supply voltage (VDD standard)		VDD2	0.3 ~ 4.0	V
Power supply voltage (VDD standard)		V0, VOUT	0.3 ~ 18.0	V
Power supply voltage (VDD standard)		V1, V2, V3, V4	V0 to 0.3	V
Operating temperature		TOPR	–40 to +85	°C
Storage temperature	Bare chip	TSTR	–55 to +125	°C

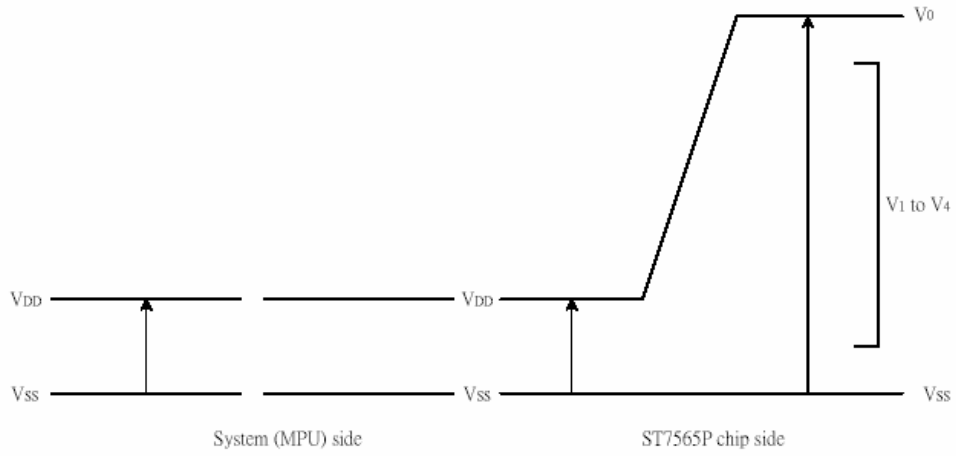


Figure 30

Notes and Cautions
1. The VDD2, V0 to V4 and VOUT are relative to the Vss = 0V reference.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that VOUT ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

PIN Assignment

Pin No	Symbol	I/O	Function
33	/CS	I	This is the chip select signal .When /CS= “ L” and CS2= “ H”,then the chip select becomes active,and data/command I/O is enabled
32	CS2	I	CS2= “ H”,ACTIVE
31	/RES	I	When /RES is set to “L” ,the setting are initialized The /RES operation is performed by the RESETB signal level

30	A0	I	Select register. 0:Instruction register (for write) Busy flag &address counter(for read) 1:Data register(for write and read).
29	/WR	I	Read/write select signal.
28	/RD	I	Operation (data read/write) enable signal.
27	D0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then D7 serves as the serial data input terminal and D6 serves as the serial clock input terminal.At this time,D0-D5 are set to high impedence. When the chip select is inactive,D0 to D7 are set to high impedance.
26	D1		
25	D2		
24	D3		
23	D4		
22	D5		
21	D6		
20	D7		
19	VDD	Supply	Power supply for logic
18	VSS	Supply	Ground.
17	VOUT	O	DC/DC voltage converter output
16	C3+	O	Capacitor3+ for internal DC/DC voltage converter
15	C1-	O	Capacitor1- for internal DC/DC voltage converter
14	C1+	O	Capacitor1+ for internal DC/DC voltage converter
13	C2+	O	Capacitor2+ for internal DC/DC voltage converter
12	C2-	O	Capacitor2- for internal DC/DC voltage converter
11	C4+	O	Capacitor4+ for internal DC/DC voltage converter
10	V4	Supply	LCD driver supply voltages.The voltage determined by LCD cell is impedangce-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship: V0>V1>V2>V3>V4>VSS When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
9	V3		
8	V2		
7	V1		

6	V0		<table><tr><td></td><td>1/65 DUTY</td></tr><tr><td>V1</td><td>1/9V0, 1/7V0</td></tr><tr><td>V2</td><td>2/9V0, 2/7V0</td></tr><tr><td>V3</td><td>7/9V0, 5/7V0</td></tr><tr><td>V4</td><td>8/9V0, 6/7V0</td></tr></table>
5	VR	I	Voltage adjustment pad.Applies voltage betweem V0 and VSS using a resistive divider
4	C86	I	C86= “ H” :6800 series MPU interface C86= “ L” :8080 series MPU interface
3	P/S	I	P/S= “ H ” :Parallel data input P/S= “ L ” :serial data input
2	/HPM	I	/HPM= “ H ” Normal mode /HPM= “ L ” High power mode
1	IRS	I	IRS= “ H ” Use the internal resisters IRS= “ L ” Donot use the internal resisters

Electrical Characteristics

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage For logic	Vdd-Vss	-	1.8	3.0	3.3	V
Supply Current For logic	Idd	-	-	-	1000	uA
Driving Current For LCD	Iee		-	-	80	uA
Driving Voltage For LCD	V0-Vss		-	-	-	V
Input Voltage H level	Vih		0.7Vdd	-	Vdd	V
Input Voltage L level	Vil		Vss	-	0.3Vdd	V

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

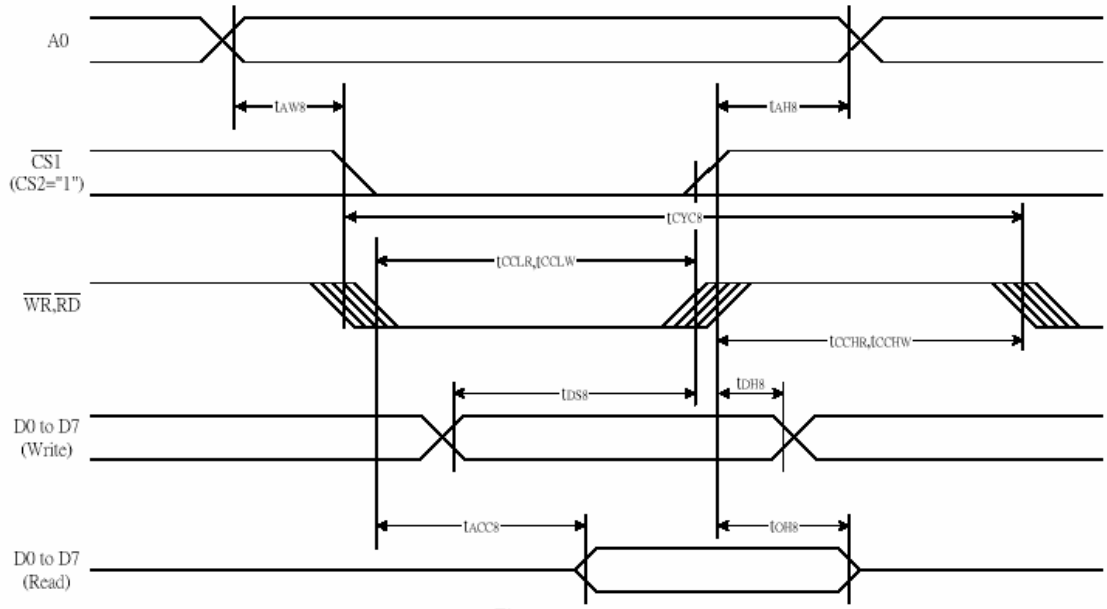


Figure 37

(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

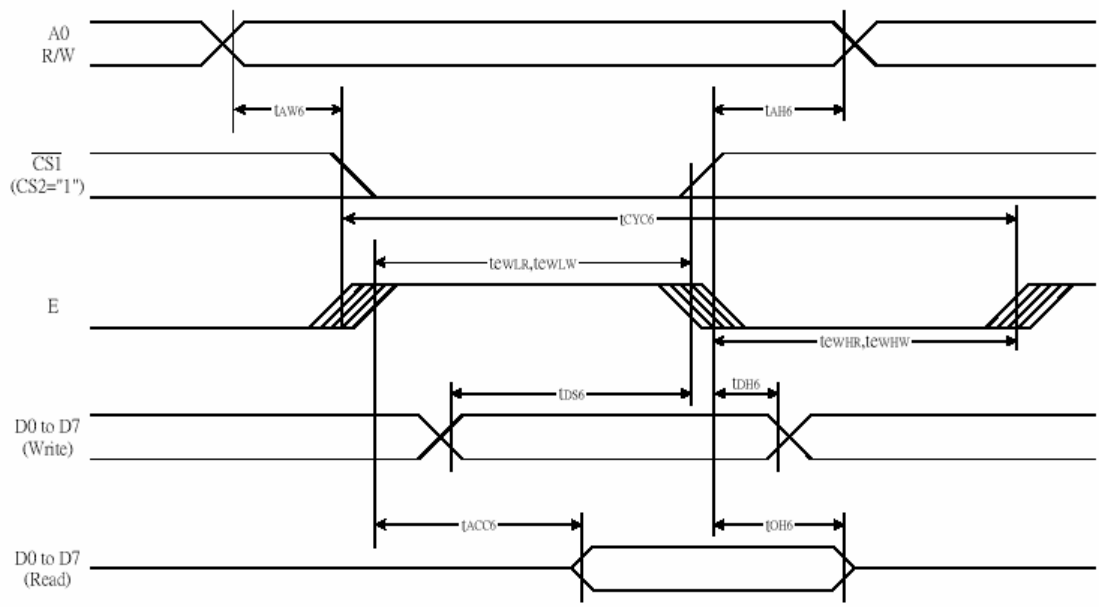
(V_{DD} = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		360	—	
Enable H pulse width (WRITE)		t_{CCHW}		280	—	
Enable L pulse width (READ)	RD	t_{CCLR}		360	—	
Enable H pulse width (READ)		t_{CCHR}		280		
WRITE Data setup time	D0 to D7	t_{DS8}		80	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being “L” (CS2 = “H”) and /WR and /RD being at the “L” level.



System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

Table 27

(V_{DD} = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

Table 28

(V_{DD} = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

(V_{DD} =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

The Serial Interface

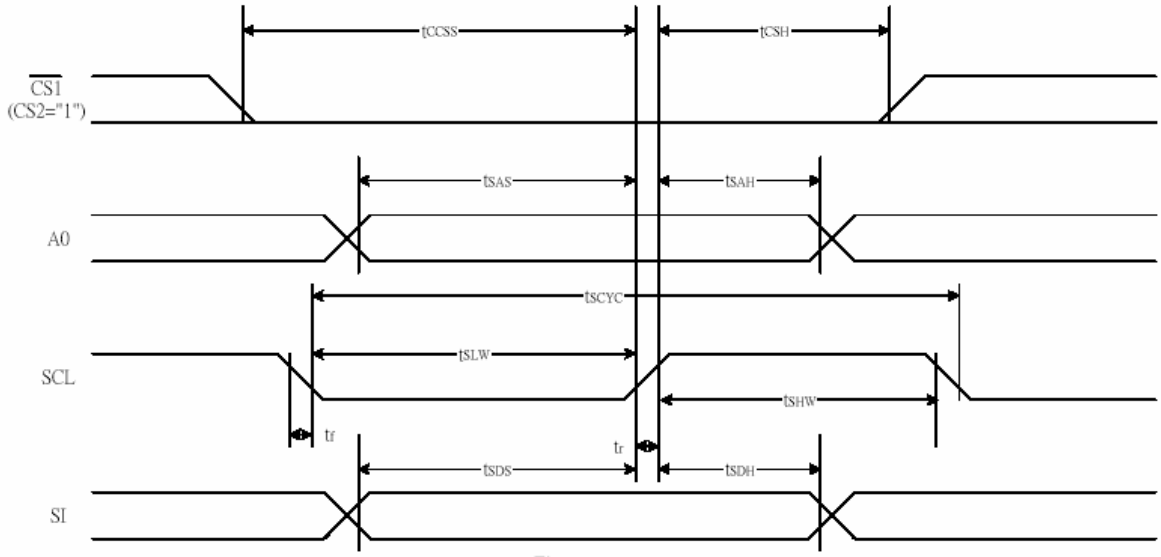


Figure 39

(VDD = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		100	—	ns
SCL "H" pulse width		T_{shw}		50	—	
SCL "L" pulse width		T_{SLW}		50	—	
Address setup time	A0	T_{SAS}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{SDH}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

Table 31

(VDD =2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		120	—	ns
SCL "H" pulse width		T_{SHW}		60	—	
SCL "L" pulse width		T_{SLW}		60	—	
Address setup time	A0	T_{SAS}		30	—	
Address hold time		T_{SAH}		20	—	
Data setup time	SI	T_{SDS}		30	—	
Data hold time		T_{SDH}		20	—	
CS-SCL time	CS	T_{CSS}		30	—	
CS-SCL time		T_{CSH}		60	—	

Table 32

(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{SCYC}		200	—	ns
SCL "H" pulse width		T_{SHW}		80	—	
SCL "L" pulse width		T_{SLW}		80	—	
Address setup time	A0	T_{SAS}		60	—	
Address hold time		T_{SAH}		40	—	
Data setup time	SI	T_{SDS}		60	—	
Data hold time		T_{SDH}		30	—	
CS-SCL time	CS	T_{CSS}		40	—	
CS-SCL time		T_{CSH}		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

IC Specification

See The Reference of Sitronix Data Book----ST7565R

Instruction Table

Table 16: Table of ST7565P Commands (Note) *: disabled data

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

Instruction Description

1. Display On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	1	1	1	**-**

D0=1 Display On
D0=0 Display Off

2. Set Display Start Line

A0	E	RW	D7	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

ST5	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

A0	E	RW	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	1	**P3**	**P2**	**P1**	**P0**

P3	**P2**	**P1**	**P0**	**Page**
0	0	0	0	0
0	0	0	1	1
.	.	.	.	.
0	1	1	1	7
1	0	0	0	8

4.Set Column Address

A0	E	RW	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	0	0	**Y7**	**Y6**	**Y5**	**Y4**
0	1	0	0	0	0	0	**Y3**	**Y2**	**Y1**	**Y0**

Y4-Y7 :Higter Bits
Y0-Y3 :Lower Bits

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status				0	0	0	0

6. Write Display Data

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7. Read Display Data

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8. ADC Select

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	0	0	**-**

D0=1 Display Reverse
D0=0 Display Normal

9. Normal/Reverse Display

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	1	1	**D**

When **D**=1 Reverse Display
D=0 Normal Display

10. Entire Display On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D=0 Nornal Display D=1 Reverse Display

11. Set LCD Bias

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	0	1	**D**

When **D**=0 Bias=1/9
D=1 Bias=1/7

12. Read-Modify-Write

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

13. End

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

14. Reset

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

15.Command Output Mode Select

A0	E	RW	D7	D6	D5	D4	**D3**	D2	D1	D0
0	1	0	1	1	0	0	**D**	*	*	*

16. Set Power Control

A0	E	RW	D7	D6	D5	D4	D3	**D2**	**D1**	**D0**
0	1	0	0	0	1	0	1	**A2**	**A1**	**A0**

When **A0**=1 Follower Circuit Is Turn On
A1=1 Regulator Circuit Is Turn On
A2=1 Booster Circuit Is Turn On

17. V0 Voltage Regulator Internal Resistor Ratio Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

18. The Electronic Volume Mode Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

19.Electronic Volume Register Set

A0	E	RW	D7	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	**SV5**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

20. Static Indicator On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	1	1	0	**D**

When **D**=0: Static Indicator Off **D**=1:Static Indicator On

21.Nop

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22.Booster Ratio Select Mode Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

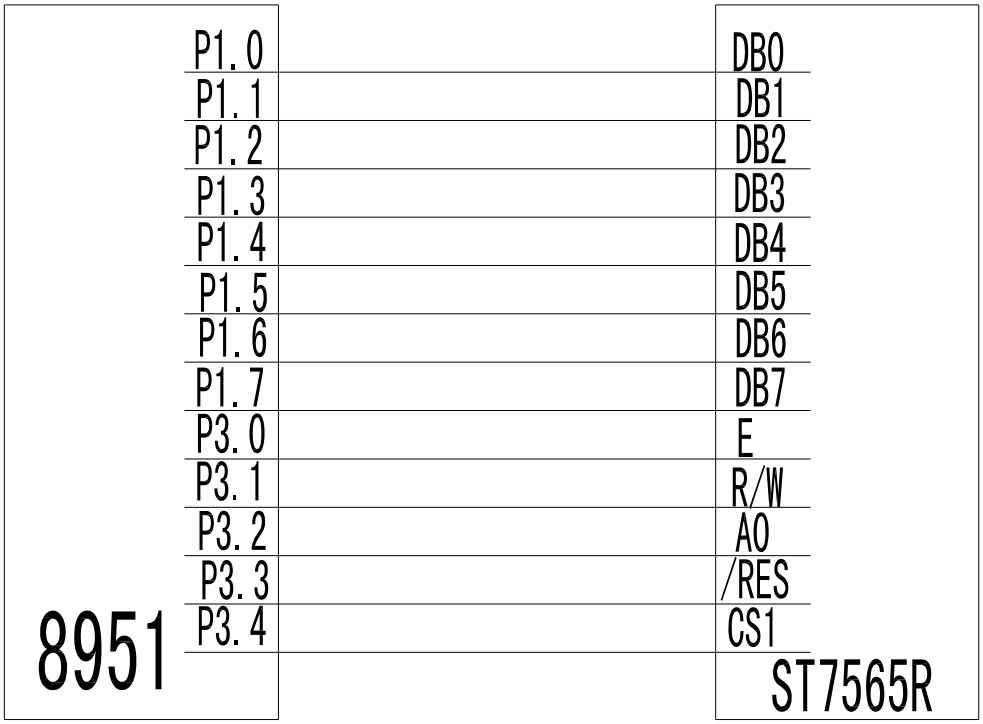
23.Booster Ratio Register Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	1	1

D1、D0=00,2x,3x,4x **D1、D0=01,5x** **D1、D0=11,6x**

Application Example

Application Circuit



Program Example

```
MOV       COM,#022H
LCALL     PR1
MOV       COM,#081H
LCALL     PR1
MOV       COM,#019H
LCALL     PR1
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
MOV       COM,#0A0H
LCALL     PR1
MOV       COM,#0C8H
LCALL     PR1
;MOV      COM,#0C0H
;LCALL    PR1
MOV       COM,#0AFH
LCALL     PR1
MOV       COM,#0A3H
LCALL     PR1
MOV       COM,#02FH
LCALL     PR1
;MOV       COM,#0F8H
;LCALL     PR1
;MOV       COM,#00H
;LCALL     PR1
;MOV      COM,#0A6H
;LCALL    PR1
;MOV      COM,#0A4H
;LCALL    PR1
;MOV      COM,#0ACH
;LCALL    PR1
;MOV      COM,#0E0H
;LCALL    PR1
;MOV      COM,#0EEH
;LCALL    PR1
;MOV     COM,#0E3H
;LCALL    PR1
MOV       COM,#040H
LCALL     PR1
```