

SPECIFICATION

128*64 Dot Matrix LCD Module

GDSC12864WM-25

(COG)

XIAMEN OCULAR LCD DEVIDES CO.,LTD.

GENERAL SPECIFICATION

Interface With Parallel MPU

Driving IC:ST7565P

Display Specification

Display Dot Matrix :128*64

Viewing Angle :6:00 Clock

Display Duty:1/65 Driving bias:1/9 Driving voltage:9.5V

Mechanical Characteristics(Unit:mm)

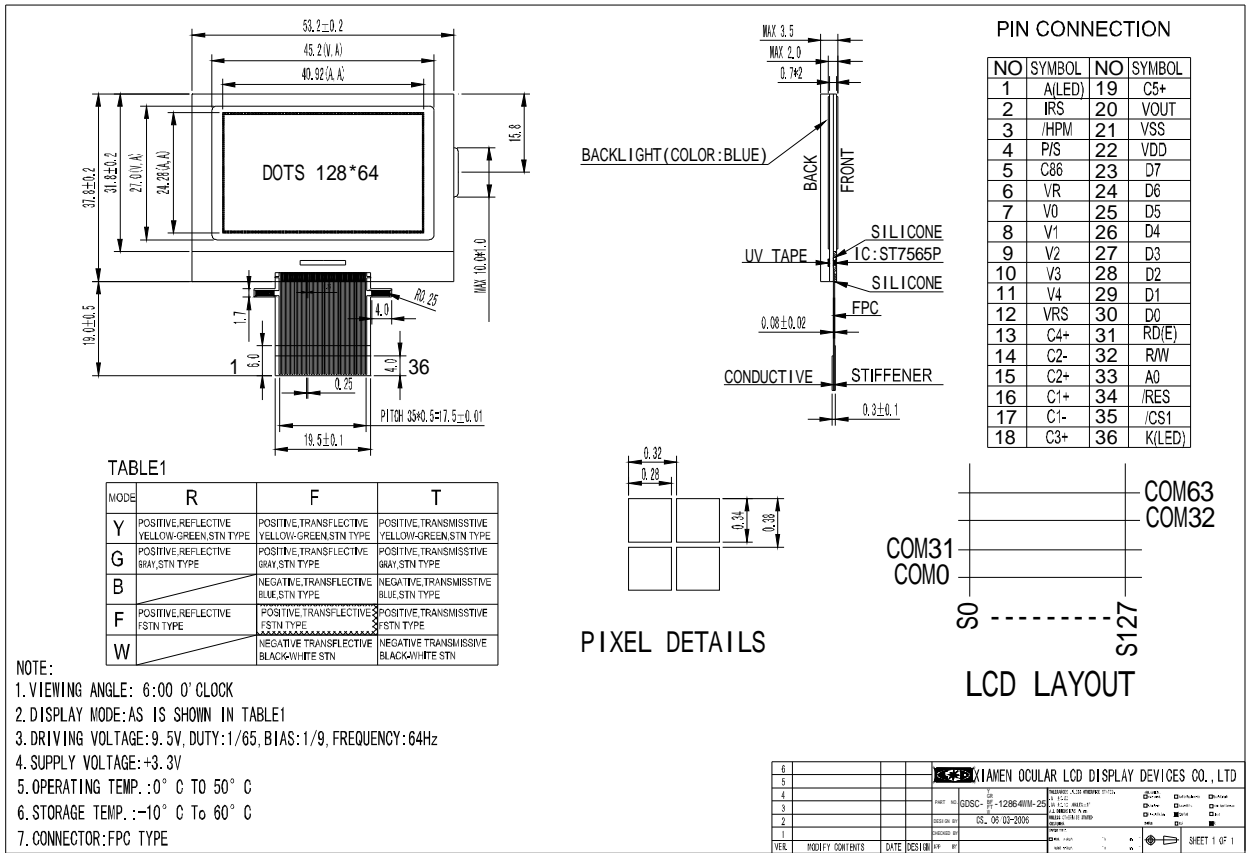
External Dimension:53.2*37.8*3.5

View Area:45.2*27.0

Dots Size:0.28*0.34

Dots Pitch:0.32*0.38

External Dimension



Absolute Maximum Ratings

Parameter	Symbol	Conditions	Unit	
Power Supply Voltage	VDD	0.3 ~ 5.0	V	
Power supply voltage (VDD standard)	VDD2	0.3 ~ 4.0	V	
Power supply voltage (VDD standard)	V0, VOUT	0.3 ~ 18.0	V	
Power supply voltage (VDD standard)	V1, V2, V3, V4	V0 to 0.3	V	
Operating temperature	TOPR	-40 to +85	°C	
Storage temperature	Bare chip	TSTR	-55 to +125	°C

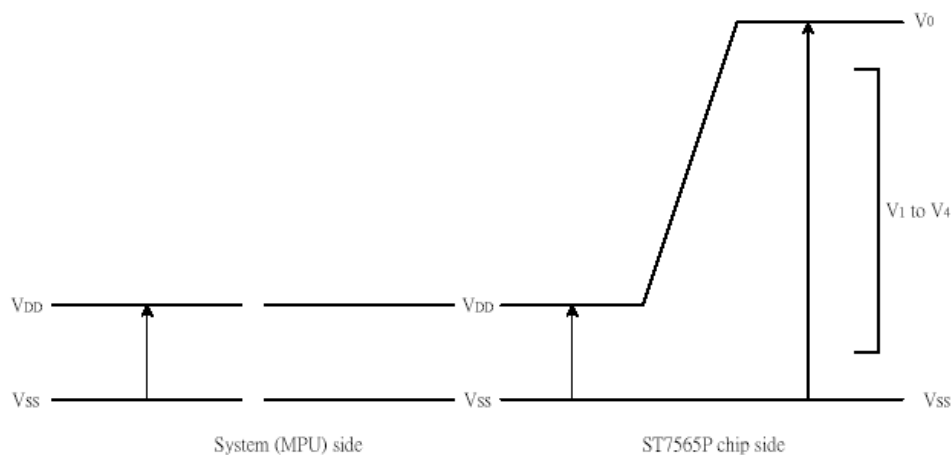


Figure 30

Notes and Cautions

1. The VDD2, V0 to V4 and VOUT are relative to the VSS = 0V reference.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that $V_{OUT} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

PIN Assignment

Pin No	Symbol	I/O	Function
36	K		LED -
35	CS1	I	This is the chip select signal .When CS1= "L" and CS2= "H",then the chip select becomes active,and data/command I/O is enabled
34	/RES	I	When /RES is set to "L" ,the setting are initialized

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			The /RES operation is performed by the RESETB signal level
33	A0	I	Select register. 0:Instruction register (for write) Busy flag & address counter(for read) 1:Data register(for write and read).
32	R/W	I	Read/write select signal.
31	E	I	Operation (data read/write) enable signal.
30	DB0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then D7 serves as the serial data input terminal and D6 serves as the serial clock input terminal.At this time,D0-D5 are set to high impedance. When the chip select is inactive,D0 to D7 are set to high impedance.
29	DB1		
28	DB2		
27	DB3		
26	DB4		
25	DB5		
24	DB6		
23	DB7		
22	VDD	Supply	Power supply for logic
21	VSS	Supply	Ground.
20	VOUT	O	DC/DC voltage converter output
19	C5+	O	Capacitor5+ for internal DC/DC voltage converter
18	C3+	O	Capacitor3+ for internal DC/DC voltage converter
17	C1-	O	Capacitor1- for internal DC/DC voltage converter
16	C1+	O	Capacitor1+ for internal DC/DC voltage converter
15	C2+	O	Capacitor2+ for internal DC/DC voltage converter
14	C2-	O	Capacitor2- for internal DC/DC voltage converter
13	C4+	O	Capacitor4+ for internal DC/DC voltage converter
12	VRS	Supply	
11	V4	Supply	LCD driver supply voltages.The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship: $V0 > V1 > V2 > V3 > V4 > VSS$ When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command
10	V3		
9	V2		

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8	V1		bias command.	
				1/65 DUTY
	V1			1/9V0, 1/7V0
7	V0			V2 2/9V0, 2/7V0
	V3			7/9V0, 5/7V0
	V4		8/9V0, 6/7V0	
6	VR			
5	C86	I	C86= "H" :6800 series MPU interface C86= "L" :8080 series MPU interface	
4	P/S	I	P/S= "H" :Parallel data input P/S= "L" :serial data input	
3	/HPM		/HPM= "H" :Normal mode /HPM= "L" :High power mode	
2	IRS		IRS= "H" :Use the internal resistors IRS= "L" :Dotnot use the internal resistors	
1	A		LED+	

Electrical Characteristics

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage For logic	Vdd-Vss	-	1.8	3.0	3.3	V
Supply Current For logic	Idd	-	-	-	1000	uA
Driving Current For LCD	Iee	-	-	-	80	uA
Driving Voltage For LCD	V0-Vss	-	-	-	-	V
Input Voltage H level	Vih	-	0.7Vdd	-	Vdd	V
Input Voltage L level	Vil	-	Vss	-	0.3Vdd	V

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The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state ($\overline{CS1} = "L"$ and $CS2 = "H"$) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when $A0 = "H"$, the data is display data, and when $A0 = "L"$ then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

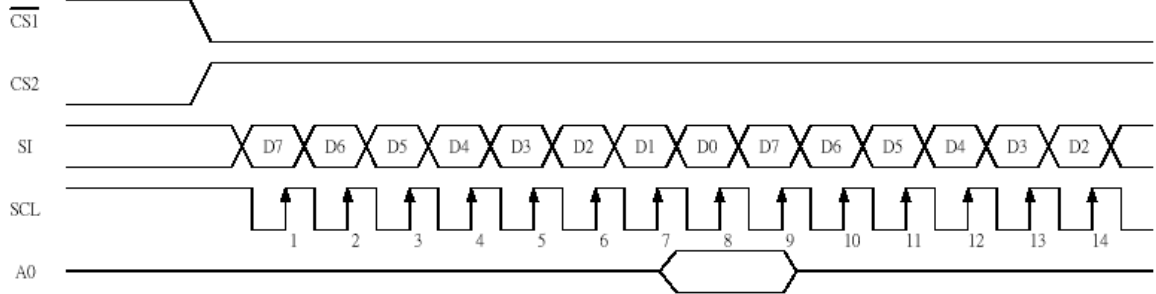


Figure 1

- * When the chip is not active, the shift registers and the counter are reset to their initial states.
- * Reading is not possible while in serial interface mode.
- * Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

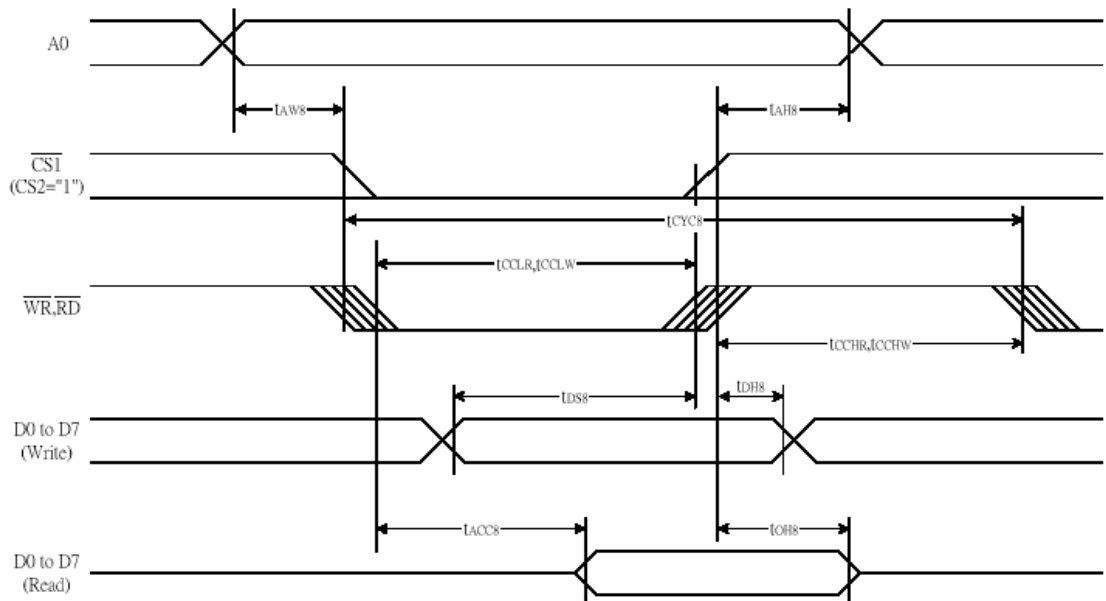


Figure 37

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(V_{DD} = 3.3V, T_a = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t _{AH8}		0	—	Ns
Address setup time		t _{AW8}		0	—	
System cycle time		t _{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t _{CCLW}		80	—	
Enable H pulse width (WRITE)		t _{CCHW}		80	—	
Enable L pulse width (READ)	RD	t _{CCLR}		140	—	
Enable H pulse width (READ)		t _{CCHR}		80	—	
WRITE Data setup time	D0 to D7	t _{DS8}		40	—	
WRITE Address hold time		t _{DH8}		0	—	
READ access time		t _{ACC8}	CL = 100 pF	—	70	
READ Output disable time		t _{OH8}	CL = 100 pF	5	50	

(V_{DD} = 2.7V, T_a = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t _{AH8}		0	—	ns
Address setup time		t _{AW8}		0	—	
System cycle time		t _{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t _{CCLW}		220	—	
Enable H pulse width (WRITE)		t _{CCHW}		180	—	
Enable L pulse width (READ)	RD	t _{CCLR}		220	—	
Enable H pulse width (READ)		t _{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t _{DS8}		40	—	
WRITE Address hold time		t _{DH8}		0	—	
READ access time		t _{ACC8}	CL = 100 pF	—	140	
READ Output disable time		t _{OH8}	CL = 100 pF	10	100	

(V_{DD} = 1.8V, T_a = 25°C)

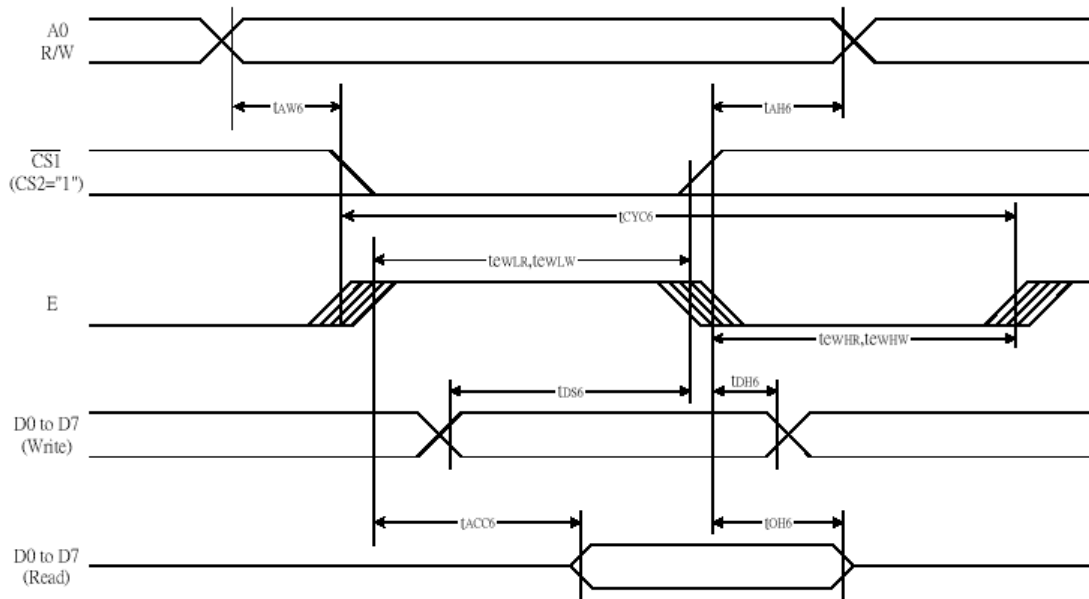
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t _{AH8}		0	—	ns
Address setup time		t _{AW8}		0	—	
System cycle time		t _{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t _{CCLW}		360	—	
Enable H pulse width (WRITE)		t _{CCHW}		280	—	
Enable L pulse width (READ)	RD	t _{CCLR}		360	—	
Enable H pulse width (READ)		t _{CCHR}		280	—	
WRITE Data setup time	D0 to D7	t _{DS8}		80	—	
WRITE Address hold time		t _{DH8}		0	—	
READ access time		t _{ACC8}	CL = 100 pF	—	240	
READ Output disable time		t _{OH8}	CL = 100 pF	10	200	

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*1 The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC6} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leq (t_{CYC6} - t_{CCLR} - t_{CCHR})$ are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.



System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

Table 27

(VDD = 3.3 V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

Table 28

(V_{DD} = 2.7V, T_a = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t _{AH6}		0	—	ns
Address setup time		t _{AW6}		0	—	
System cycle time		t _{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t _{EWLW}		220	—	
Enable H pulse width (WRITE)		t _{EWHW}		180	—	
Enable L pulse width (READ)	RD	t _{EWLR}		220	—	
Enable H pulse width (READ)		t _{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t _{DS6}		40	—	
WRITE Address hold time		t _{DH6}		0	—	
READ access time		t _{ACC6}	CL = 100 pF	—	140	
READ Output disable time		t _{OH6}	CL = 100 pF	10	100	

(V_{DD} = 1.8V, T_a = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t _{AH6}		0	—	ns
Address setup time		t _{AW6}		0	—	
System cycle time		t _{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t _{EWLW}		360	—	
Enable H pulse width (WRITE)		t _{EWHW}		280	—	
Enable L pulse width (READ)	RD	t _{EWLR}		360	—	
Enable H pulse width (READ)		t _{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t _{DS6}		80	—	
WRITE Address hold time		t _{DH6}		0	—	
READ access time		t _{ACC6}	CL = 100 pF	—	240	
READ Output disable time		t _{OH6}	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (t_r + t_f) ≤ (t_{CYC6} – t_{EWLW} – t_{EWHW}) for (t_r + t_f) ≤ (t_{CYC6} – t_{EWLR} – t_{EWHR}) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{EWLW} and t_{EWLR} are specified as the overlap between CS1 being "L" (CS2 = "H") and E.

The Serial Interface

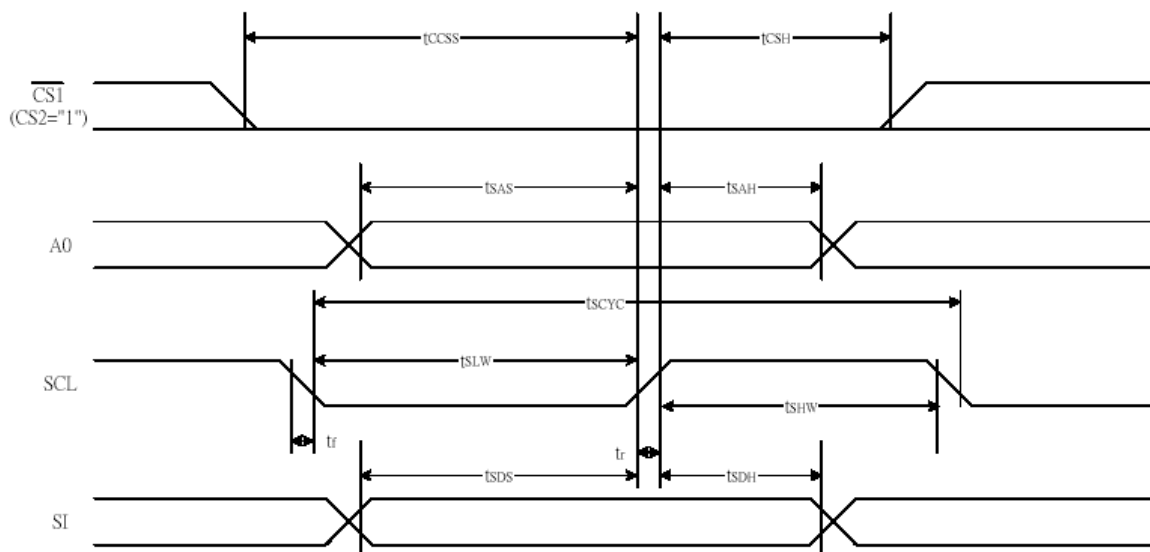


Figure 39

(VDD = 3.3V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		100	—	ns
SCL "H" pulse width		T_{shw}		50	—	
SCL "L" pulse width		T_{slw}		50	—	
Address setup time	A0	T_{sas}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{sdh}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

Table 31

(VDD = 2.7V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		120	—	ns
SCL "H" pulse width		T_{shw}		60	—	
SCL "L" pulse width		T_{slw}		60	—	
Address setup time	A0	T_{sas}		30	—	
Address hold time		T_{sah}		20	—	
Data setup time	SI	T_{sds}		30	—	
Data hold time		T_{sdh}		20	—	
CS-SCL time	CS	T_{css}		30	—	
CS-SCL time		T_{csh}		60	—	

Table 32

(V_{DD} = 1.8V, T_a = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T _{SCYC}		200	—	ns
SCL "H" pulse width		T _{SHW}		80	—	
SCL "L" pulse width		T _{SLW}		80	—	
Address setup time	A0	T _{SAS}		60	—	
Address hold time		T _{SAH}		40	—	
Data setup time	SI	T _{SDS}		60	—	
Data hold time		T _{SDH}		30	—	
CS-SCL time	CS	T _{CSS}		40	—	
CS-SCL time		T _{CSSH}		100	—	

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

IC Specification

See The Reference of Sitronix Data Book----ST7565P

Instruction Table

Table 16: Table of ST7565P Commands

(Note) *: disabled data

Command	Command Code										Function	
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1		D0
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address					1	Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data							Writes to the display RAM	
(7) Display data read	1	0	1	Read data							Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	Sets the LCD display normal/reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode		Select internal power supply operating mode	
(17) V ₀ voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio		Select internal resistor ratio(Rb/Ra) mode	
(18) Electronic volume mode set Electronic volume register set	0	1	0	1	0	0	0	0	0	0	1	Set the V ₀ output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1	0	1	0	1	1	0	0	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

Instruction Description

1. Display On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	-

D0=1 Display On

D0=0 Display Off

2. Set Display Start Line

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
.
0	1	1	1	7
1	0	0	0	8

4. Set Column Address

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	Y7	Y6	Y5	Y4
0	1	0	0	0	0	0	Y3	Y2	Y1	Y0

Y4-Y7 :Higher Bits

Y0-Y3 :Lower Bits

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Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status				0	0	0	0

6. Write Display Data

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7. Read Display Data

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8. ADC Select

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	-

D0=1 Display Reverse

D0=0 Display Normal

9. Normal/Reverse Display

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When **D**=1 Reverse Display

D=0 Normal Display

10. Entire Display On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When **D**=0 Normal Display **D**=1 Reverse Display

11. Set LCD Bias

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

When **D**=0 Bias=1/9

D=1 Bias=1/7

12. Read-Modify-Write

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

13. End

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

14. Reset

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

15. Command Output Mode Select

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

16. Set Power Control

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When **A0**=1 Follower Circuit Is Turn On

A1=1 Regulator Circuit Is Turn On

A2=1 Booster Circuit Is Turn On

17. V0 Voltage Regulator Internal Resistor Ratio Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

18. The Electronic Volume Mode Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

19. Electronic Volume Register Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	SV5	SV4	SV3	SV2	SV1	SV0

20. Static Indicator On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

When **D**=0: Static Indicator Off **D**=1: Static Indicator On

21.Nop

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22.Booster Ratio Select Mode Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

23.Booster Ratio Register Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	1	1

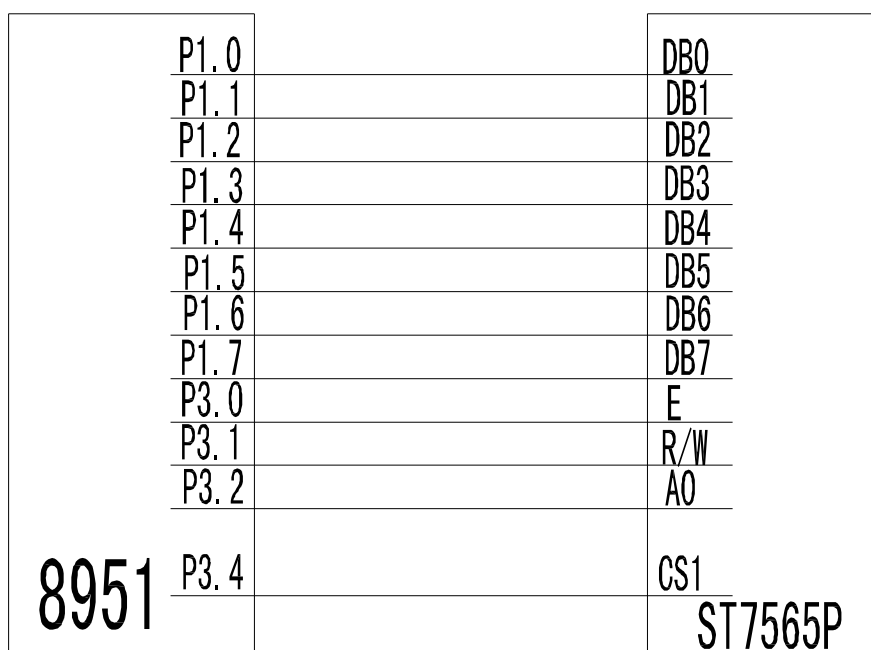
D1、D0=00,2x,3x,4x

D1、D0=01,5x

D1、D0=11,6x

Application Example

Application Circuit



COMPANY PROFILE

XIAMEN OCULAR LCD DEVIDES CO.,LTD. Was formed in 1992. Our company is a joint-venture specializing in manufacturing all kinds of Liquid Crystal Displays. We design and massproduce Touch Panel,LED,COG, the digital segment, dot matrix LCD panels, and modules in TN,HTN and STN types using the advanced and whole facilities and soft-ware technology.

Most of our products are customer_mode. Xiamen Ocular's LCDs now have a good sale not only in domextic China,but also in America,Europe and East_south Aisa.These LCDs were widely used in the display of instruments,clocks,telecommunication equipments,calcuators,air conditioner controllers and AV systems.

Based upon the reliable high quality, reasonable price and quick delivery, Xiamen Ocular will sever all customers wholeheartedly.

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