SPECIFICATION

128*64 Dot Matrix LCD Module

GDSC12864WM-20

(COG)

XIAMEN OCULAR LCD DEVIDES CO.,LTD.

GENERAL SPECIFICATION

Interace With Parallel MPU

Driving IC:S1D15605

Display Specification

Display Dot Matrix :128*64

Viewing Angle :6:00 Clock

Display Duty:1/65 Driving bias:1/9 Driving voltage:8.9V

Mechanical Characteristics(Unit:mm)

Extenal Dimension:89.7*49.8*6.0

View Area:66.8*35.5

Dots Size:0.48*0.48

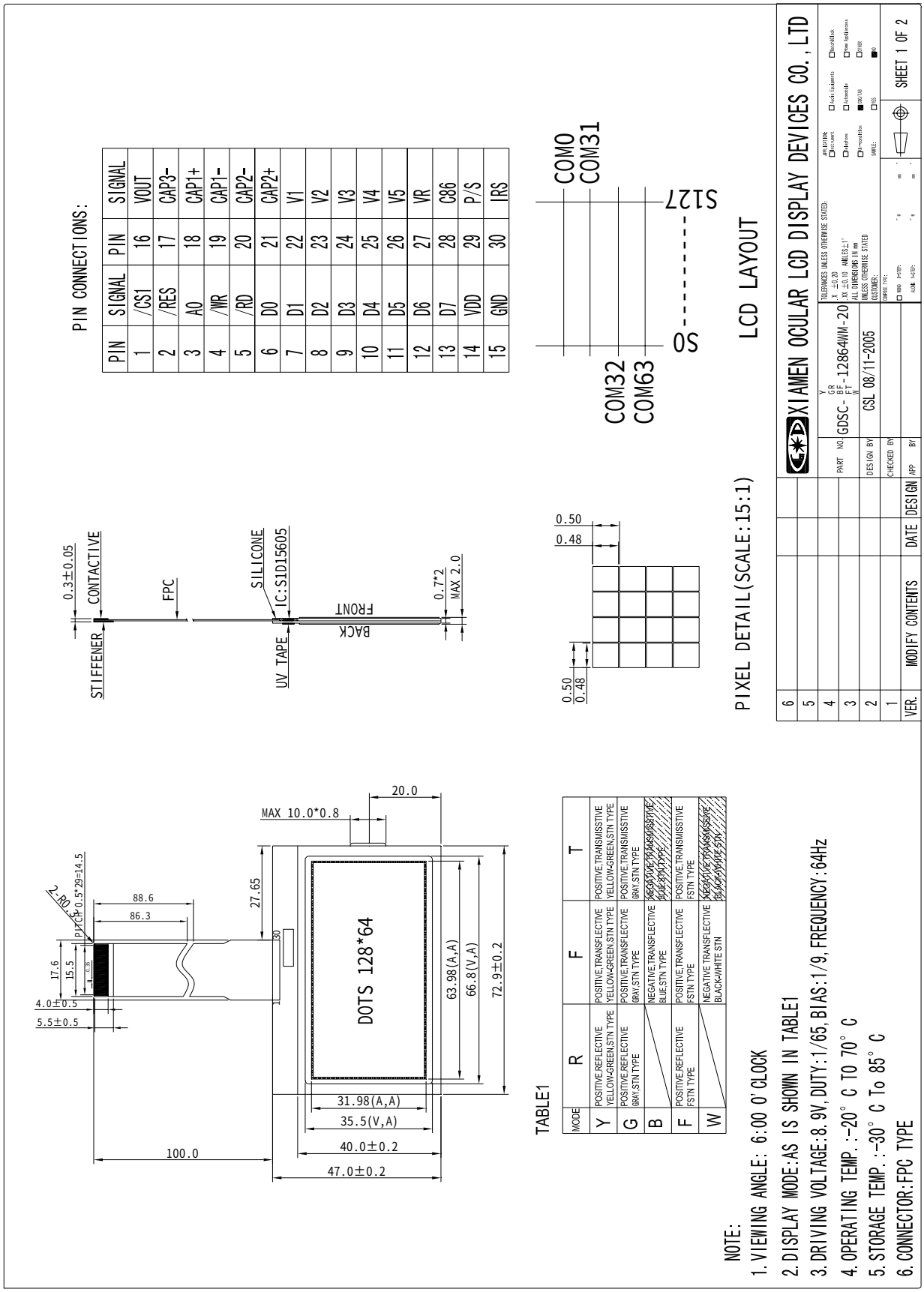
Dots Pitch:0.50*0.50

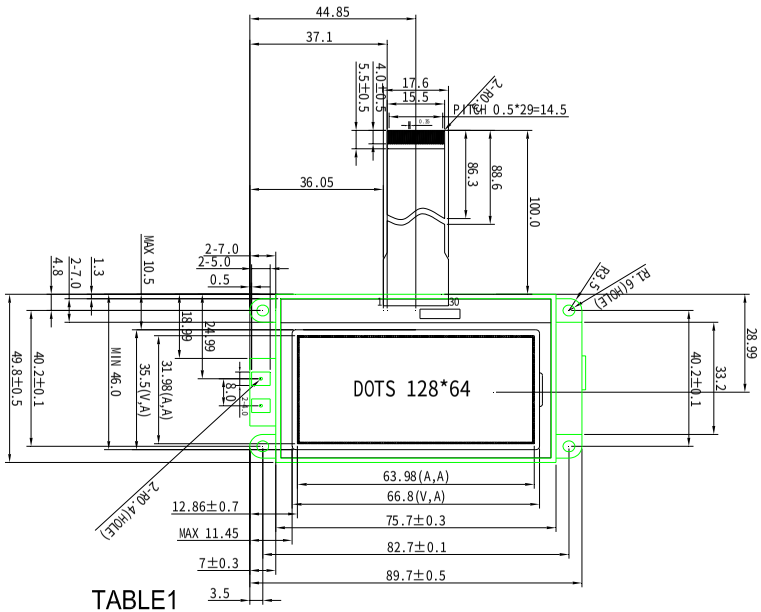
Led Supply Voltage:3.0-3.5V

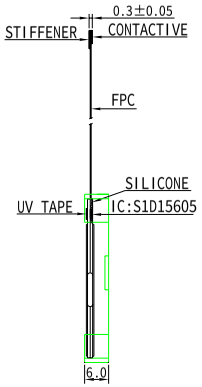
Led Supply Voltage:45mA

Led Color:White

External Dimension







PIN CONNECTIONS

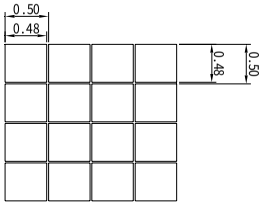
PIN	SIGNAL	PIN	SIGNAL
1	/CS1	16	VOUT
2	/RES	17	CAP3-
3	A0	18	CAP1+
4	/WR	19	CAP1-
5	/RD	20	CAP2-
6	D0	21	CAP2+
7	D1	22	V1
8	D2	23	V2
9	D3	24	V3
10	D4	25	V4
11	D5	26	V5
12	D6	27	VR
13	D7	28	C86
14	VDD	29	P/S
15	GND	30	IRS

TABLE1

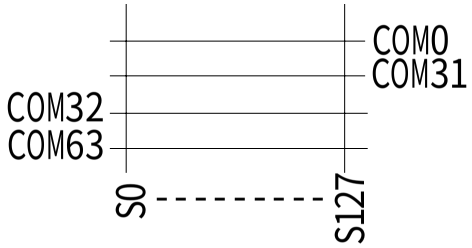
MODE	R	F	T
Y	POSITIVE,REFLECTIVE YELLOW-GREEN,STN TYPE	POSITIVE,TRANSFLECTIVE YELLOW-GREEN,STN TYPE	POSITIVE,TRANSMISSTIVE YELLOW-GREEN,STN TYPE
G	POSITIVE,REFLECTIVE GRAY,STN TYPE	POSITIVE,TRANSFLECTIVE GRAY,STN TYPE	POSITIVE,TRANSMISSTIVE GRAY,STN TYPE
B		NEGATIVE,TRANSFLECTIVE BLUE,STN TYPE	NEGATIVE,TRANSMISSTIVE BLUE,STN TYPE
F	POSITIVE,REFLECTIVE FSTN TYPE	POSITIVE,TRANSFLECTIVE FSTN TYPE	POSITIVE,TRANSMISSTIVE FSTN TYPE
W		NEGATIVE TRANSFLECTIVE BLACK-WHITE STN	NEGATIVE TRANSMISSIVE BLACK-WHITE STN

NOTE:

1. VIEWING ANGLE: 6:00 O'CLOCK
2. DISPLAY MODE:AS IS SHOWN IN TABLE1
3. LED DRIVING VOLTAGE/CURRENT: 3.0-3.5V/45-60mA
4. LED COLOR:WHITE
5. DRIVING VOLTAGE:8.9V, DUTY:1/65, BIAS:1/9, FREQUENCY:64Hz
6. OPERATING TEMP.:-20° C TO 70° C
7. STORAGE TEMP.:-30° C To 85° C
8. CONNECTOR:FPC TYPE



PIXEL DETAIL(SCALE:15:1)



LCD LAYOUT

VER.	MODIFY CONTENTS	DATE	DESIGN
6			
5			
4			
3			
2			
1			

XIAMEN OCULAR LCD DISPLAY DEVICES CO.,LTD

PART NO: GDSC-YGRBFTW-12864WM-20

DESIGN BY: CSL 08/11-2005

CHECKED BY:

TOLERANCES UNLESS OTHERWISE STATED:
X ±0.00
XX ±0.10 ANGLES±1°
ALL DIMENSIONS IN mm
UNLESS OTHERWISE STATED
CUSTOMER:

APPLICATION: Instrument, Audio Equipments, Watch&Clock, Telephone, Automobile, Home Appliances, Air-condition, COG/TAB, OTHER
SAMPLE: YES

COMPOSE TYPE: MONO X-STEP: Y-STEP:

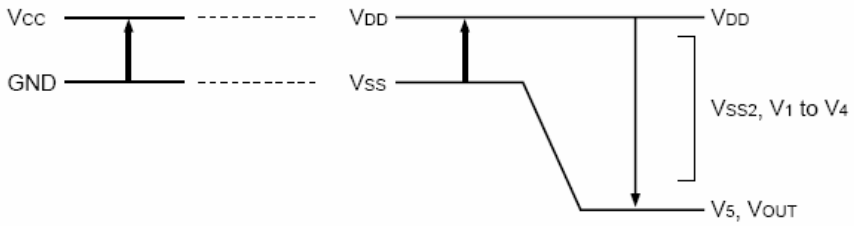
PIN assignment

Pin	Symbol	Function
1	**/CS1**	This is the chip select signal .When CS1=“ L” and CS2=“ H”,then the chip select becomes active,and data/command I/O is enabled
2	**/RES**	When /RES is set to “L” ,the setting are initialized The /RES operation is performed by the /RES signal level
3	**A0**	Select register. 0:Instruction register (for write) Busy flag &address counter(for read) 1:Data register(for write and read).
4	**/WR**	Read/write select signal.
5	**/RD**	Operation (data read/write) enable signal.
6	**DB0**	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then DB7 serves as the serial data input terminal and DB6 serves as the serial clock input terminal.At this time,DB0-DB5 are set to high impedence. When the chip select is inactive,DB0 to DB7 are set to high impedance.
7	**DB1**	
8	**DB2**	
9	**DB3**	
10	**DB4**	
11	**DB5**	
12	**DB6**	
13	**DB7**	
14	**VDD**	Power supply for logic
15	**VSS**	Ground.
16	**VOUT**	DC/DC voltage converter output
17	**CAP3-**	Capacitor3- for internal DC/DC voltage converter
18	**CAP1+**	Capacitor1+ for internal DC/DC voltage converter
19	**CAP1-**	Capacitor1- for internal DC/DC voltage converter
20	**CAP2-**	Capacitor2- for internal DC/DC voltage converter
21	**CAP2+**	Capacitor2+ for internal DC/DC voltage converter
22	**V1**	LCD driver supply voltages.The voltage determined by LCD cell is impedangce-converted by a resistive driver or an operation amplifier for application .Voltages should be the following
23	**V2**	
24	**V3**	

<table>
<tr><td>25</td><td>V4</td><td rowspan="2">relationship:
V0>V1>V2>V3>V4>VSS
When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
<table>
<tr><td>LCD BIAS</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/5BIAS</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 BIAS</td><td>5/6V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 BIAS</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 BIAS</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 BIAS</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>26</td><td>V5</td></tr>
<tr><td>27</td><td>VR</td><td>Voltage adjustment pad.Applies voltage betweem V5 and VSS using a resistive divider</td></tr>
<tr><td>28</td><td>C86</td><td>C86=“ H” :6800 series MPU interface
C86=“ L” :8080 series MPU interface</td></tr>
<tr><td>29</td><td>PS</td><td>P/S=“ H ” :Parallel data input
P/S=“ L ” :serial data input</td></tr>
<tr><td>30</td><td>IRS</td><td>IRS=“ H ” Use the internal resisters
IRS=“ L ”Donot use the internal resisters</td></tr>
</table>

Absolute Maximun Ratings

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +7.0	V
Power supply voltage (2) (V_{DD} standard)	With Triple step-up With Quad step-up	V_{SS2}	–7.0 to +0.3 –6.0 to +0.3 –4.5 to +0.3	V
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	–18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP Bare chip	T_{STR}	–55 to +100 –55 to +125	°C



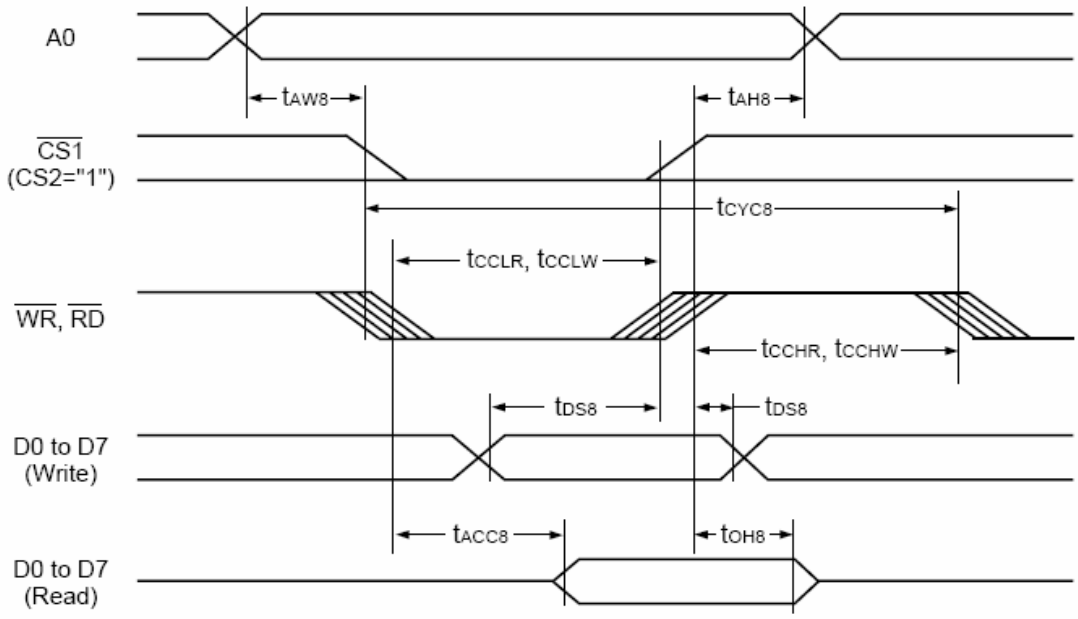
Notes and Cautions
1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

Electrical Characteristics

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage For logic	Vdd-Vss	-	1.8	-	5.5	V
Supply Current For logic	Idd	-	-	-	1000	uA
Driving Current For LCD	Iee		-	-	80	uA
Driving Voltage For LCD	V0-Vss		-	-	-	V
Input Voltage H level	Vih		0.7Vdd	-	Vdd	V
Input Voltage L level	Vil		Vss	-	0.3Vdd	V

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



(VDD = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		166	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	ns
Data setup time	D0 to D7	t_{DS8}		30	—	ns
Address hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	70	ns
Output disable time		t_{OH8}		5	50	ns

(VDD = 2.7 V to 4.5 V, Ta = –40 to 85°C)

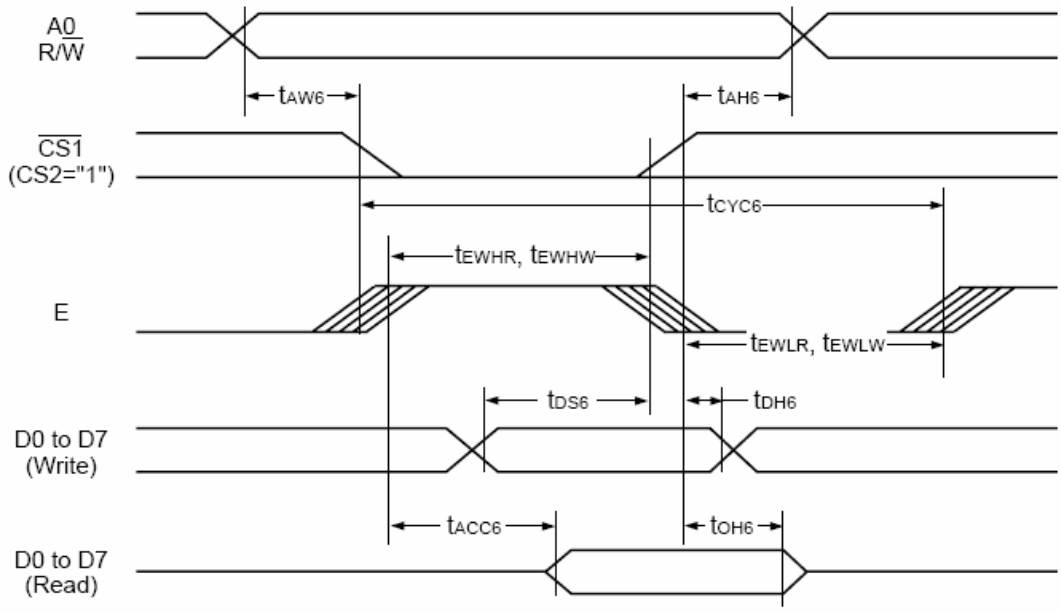
Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		300	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time Address setup time	A0	t_{AH8} t_{AW8}		0 0	— —	ns ns
System cycle time	A0	t_{CYC8}		1000	—	ns
Control L pulse width ($\overline{WR}$) Control L pulse width ($\overline{RD}$) Control H pulse width ($\overline{WR}$) Control H pulse width ($\overline{RD}$)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		120 240 120 120	— — — —	ns ns ns ns
Data setup time Address hold time	D0 to D7	t_{DS8} t_{DH8}		80 30	— —	ns ns
$\overline{RD}$ access time Output disable time		t_{ACC8} t_{OH8}	C_L = 100 pF	— 10	280 200	ns ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

System Bus Read/Write Characteristics 2 (6800 Series MPU)



(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		166	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		30 10	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	70 50	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		70 30	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		30 30	— —	ns ns

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		300	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	140 100	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		120 60	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		60 60	— —	ns ns

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		1000	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	280 200	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		240 120	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		120 120	— —	ns ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

IC Specification

See The Reference of EPSON Data Book----S1D15605

Instruction Table

	Command	Command Code A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio SED1565*** ..... 0: 1/9, 1: 1/7 SED1566*** /SED1568*** /SED1569*** ..... 0: 1/8, 1: 1/6 SED1567*** 0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V_5 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note) *: disabled data

Instruction Description

1. Display On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	1	1	1	**-**

D0=1 Display On
D0=0 Display Off

2. Set Display Start Line

A0	E	RW	D7	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

ST5	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

A0	E	RW	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	1	**P3**	**P2**	**P1**	**P0**

P3	**P2**	**P1**	**P0**	**Page**
0	0	0	0	0
0	0	0	1	1
.	.	.	.	.
0	1	1	1	7
1	0	0	0	8

4.Set Column Address

A0	E	RW	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	0	0	**Y7**	**Y6**	**Y5**	**Y4**
0	1	0	0	0	0	0	**Y3**	**Y2**	**Y1**	**Y0**

Y4-Y7 :Higter Bits
Y0-Y3 :Lower Bits

Y7	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**	**Column Address**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status				0	0	0	0

6. Write Display Data

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7. Read Display Data

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8. ADC Select

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	0	0	**-**

D0=1 Display Reverse
D0=0 Display Normal

9. Normal/Reverse Display

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	1	1	**D**

When **D**=1 Reverse Display
D=0 Normal Display

10. Entire Display On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D=0 Nornal Display D=1 Reverse Display

11. Set LCD Bias

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	0	1	**D**

When **D**=0 Bias=1/9
D=1 Bias=1/7

12. Read-Modify-Write

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

13. End

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

14. Reset

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

15.Command Output Mode Select

A0	E	RW	D7	D6	D5	D4	**D3**	D2	D1	D0
0	1	0	1	1	0	0	**D**	*	*	*

16. Set Power Control

A0	E	RW	D7	D6	D5	D4	D3	**D2**	**D1**	**D0**
0	1	0	0	0	1	0	1	**A2**	**A1**	**A0**

When **A0**=1 Follower Circuit Is Turn On
A1=1 Regulator Circuit Is Turn On
A2=1 Booster Circuit Is Turn On

17. V0 Voltage Regulator Internal Resistor Ratio Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

18. The Electronic Volume Mode Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

19.Electronic Volume Register Set

A0	E	RW	D7	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	**SV5**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

20. Static Indicator On/Off

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	1	1	0	**D**

When **D**=0: Static Indicator Off **D**=1:Static Indicator On

21.Nop

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22.Booster Ratio Select Mode Set

A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

23.Booster Ratio Register Set

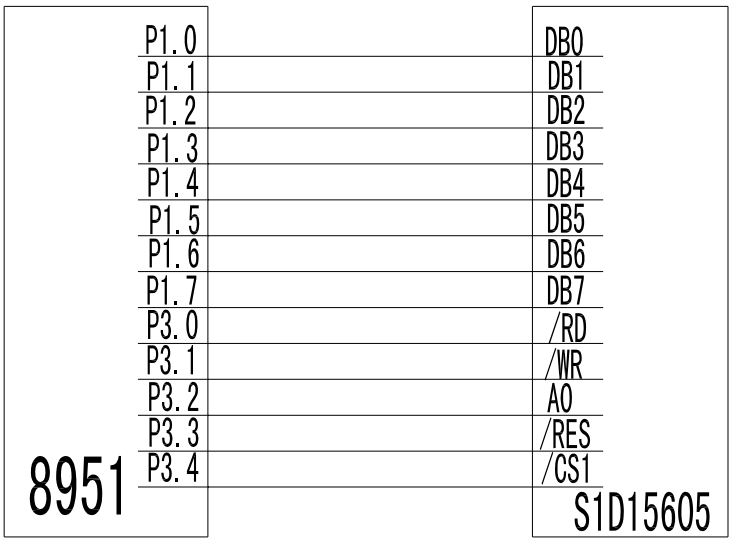
A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1

0	1	0	0	0	0	0	0	0	1	1

D1、D0=00,2x,3x,4x **D1、D0=01,5x** **D1、D0=11,6x**

Application Example

Application Circuit



COMPANY PROFILE

XIAMEN OCULAR LCD DEVIDES CO.,LTD. Was formed in 1992. Our company is a joint-venture specializing in manufacturing all kinds of Liquid Crystal Displays. We design and massproduce Touch Panel,LED,COG, the digital segment, dot matrix LCD panels, and modules in TN,HTN and STN types using the advanced and whole facilities and soft-ware technology.

Most of our products are customer_mode. Xiamen Ocular's LCDs now have a good sale not only in domextic China,but also in America,Europe and East_south Aisa.These LCDs were widely used in the display of instruments,clocks,telecommunication equipments,calcuators,air conditioner controllers and AV systems.

Based upon the reliable high quality, reasonable price and quick delivery, Xiamen Ocular will sever all customers wholeheartedly.

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