SPECIFICATION

128*64 Dot Matrix LCD Module

GDSC-12864BM-02

(COG)

XIAMEN OCULAR LCD DEVIDES CO.,LTD.

General Specification

Driving IC S6B0724A

Interace With **Paraller** MPU

Display Dot Matrix :**128*64**

Display Mode:Positive/Transflective/STN Type(YG)

Viewing angle :**6:00** Clock

Display Duty:**1/65** Driving Bias:**1/9** Driving Voltage:**9.5V**

Mechanical Characteristics(Unit:mm)

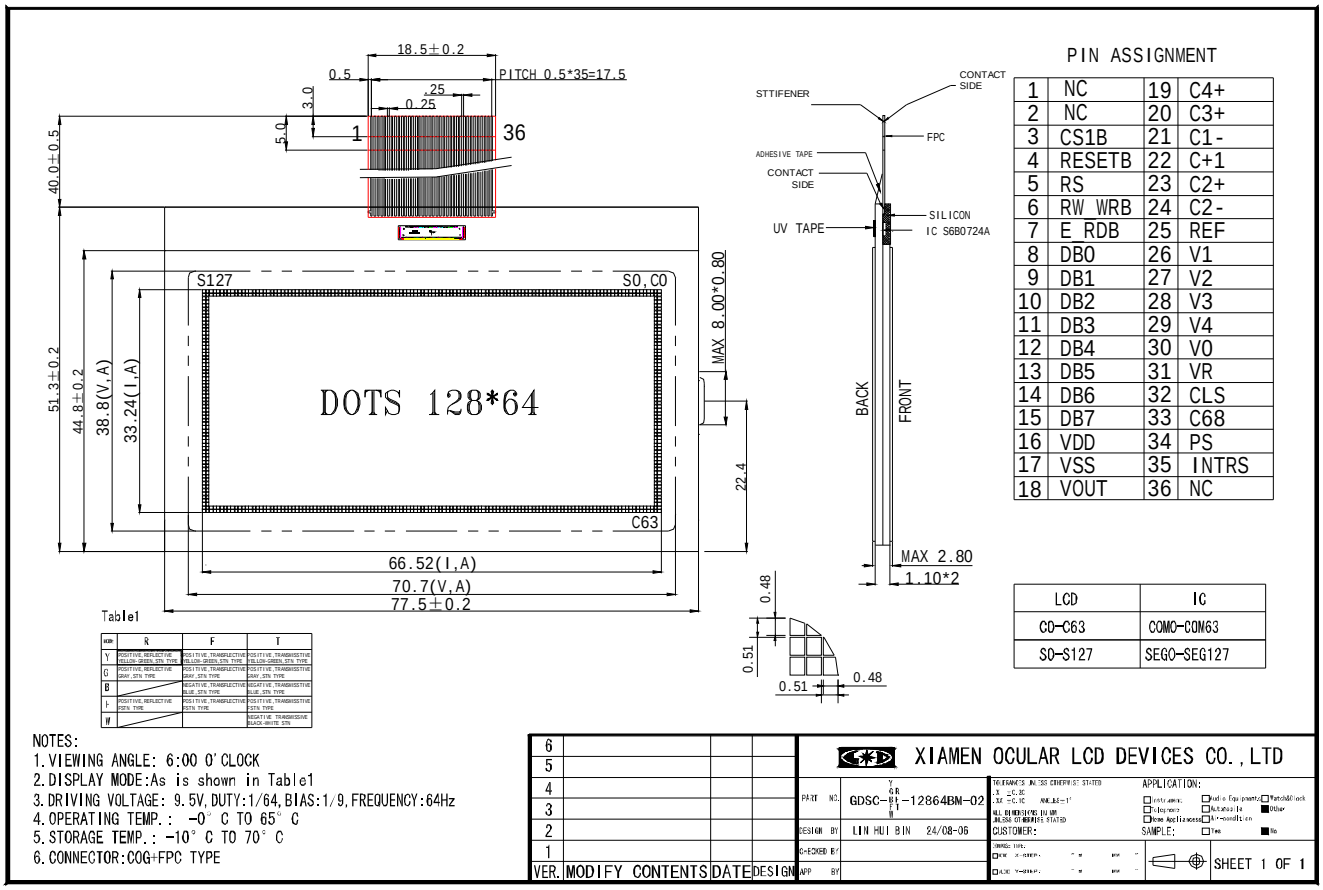
Extenal Dimension:**77.5*51.3*2.8**

View Area:**66.52*33.24**

Dots Size:**0.48*0.48**

Dots Pitch:0.52*0.52

External Dimension



Absolute Maximum Ratings

Item	Symbol	Standard			Unit
Power supply voltage	V_{DD}-V_{SS}	0	-	5.5	V
Input voltage	VIN	VSS	-	VDD	
Operating temperature range	T_A	-20	-	+70	℃
Storage temperature range	T_{STO}	-30	-	+80	

*****Wide temperature range is available

Interface Pin Description

Pin No	Symbol	I/O	Function
1	NC		No Connected
2	CL	I/O	Display clock input/output pin
3	CS1B	I	This is the chip select signal .When CS1B= "L" and CS2= "H",then the chip select becomes active,and data/command I/O is enabled
4	RESETB	I	When RESETB is set to "L",the setting are initialized The RESETB operation is performed by the RESETB signal level
5	RS	I	Select register. 0:Instruction register (for write) Busy flag &address counter(for read) 1:Data register(for write and read).
6	RW-WRB	I	Read/write select signal.
7	E-RDB	I	Operation (data read/write) enable signal.
8	DB0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then D7 serves as the serial data input terminal and D6 serves as the serial clock input terminal.At this time,D0-D5 are set to high impedence. When the chip select is inactive,D0 to D7 are set to high impedance.
9	DB1		
10	DB2		
11	DB3		
12	DB4		
13	DB5		
14	DB6		
15	DB7		
16	VDD	Supply	Power supply for logic
17	VSS	Supply	Ground.
18	VOUT	O	DC/DC voltage converter output

<table>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>19</td><td>C4+</td><td>O</td><td>Capacitor4+ for internal DC/DC voltage converter</td></tr>
<tr><td>20</td><td>C3+</td><td>O</td><td>Capacitor3+ for internal DC/DC voltage converter</td></tr>
<tr><td>21</td><td>C1-</td><td>O</td><td>Capacitor1- for internal DC/DC voltage converter</td></tr>
<tr><td>22</td><td>C1+</td><td>O</td><td>Capacitor1+ for internal DC/DC voltage converter</td></tr>
<tr><td>23</td><td>C2+</td><td>O</td><td>Capacitor2+ for internal DC/DC voltage converter</td></tr>
<tr><td>24</td><td>C2-</td><td>O</td><td>Capacitor2- for internal DC/DC voltage converter</td></tr>
<tr><td>25</td><td>REF</td><td>I</td><td>Select the external V_{REF} voltage via VEXT</td></tr>
<tr><td>26
27
28
29
30</td><td>V1
V2
V3
V4
V0</td><td>Supply</td><td>LCD driver supply voltages.The voltage determined by LCD cell is impedangce-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship:
V0>V1>V2>V3>V4>VSS
When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
<table>
<tr><td>LCD BIAS</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/5BIAS</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 BIAS</td><td>5/6V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 BIAS</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 BIAS</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 BIAS</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>31</td><td>VR</td><td>I</td><td>Voltage adjustment pad.Applies voltage betweem V0 and VSS using a resistive divider</td></tr>
<tr><td>32</td><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable/disable select pin</td></tr>
<tr><td>33</td><td>C68</td><td>I</td><td>C68=“H” :6800 series MPU interface
C68=“L” :8080 series MPU interface</td></tr>
<tr><td>34</td><td>PS</td><td>I</td><td>P/S=“H” :Parallel data input
P/S=“L” :serial data input</td></tr>
<tr><td>35</td><td>INTRS</td><td>I</td><td>Internal resistor select pin
INTRS=“H”:use the internal resistors
INTRS=“L”:use the external resistors</td></tr>
<tr><td>36</td><td>NC</td><td></td><td>No Connected</td></tr>
</table>

Electrical Characteristics

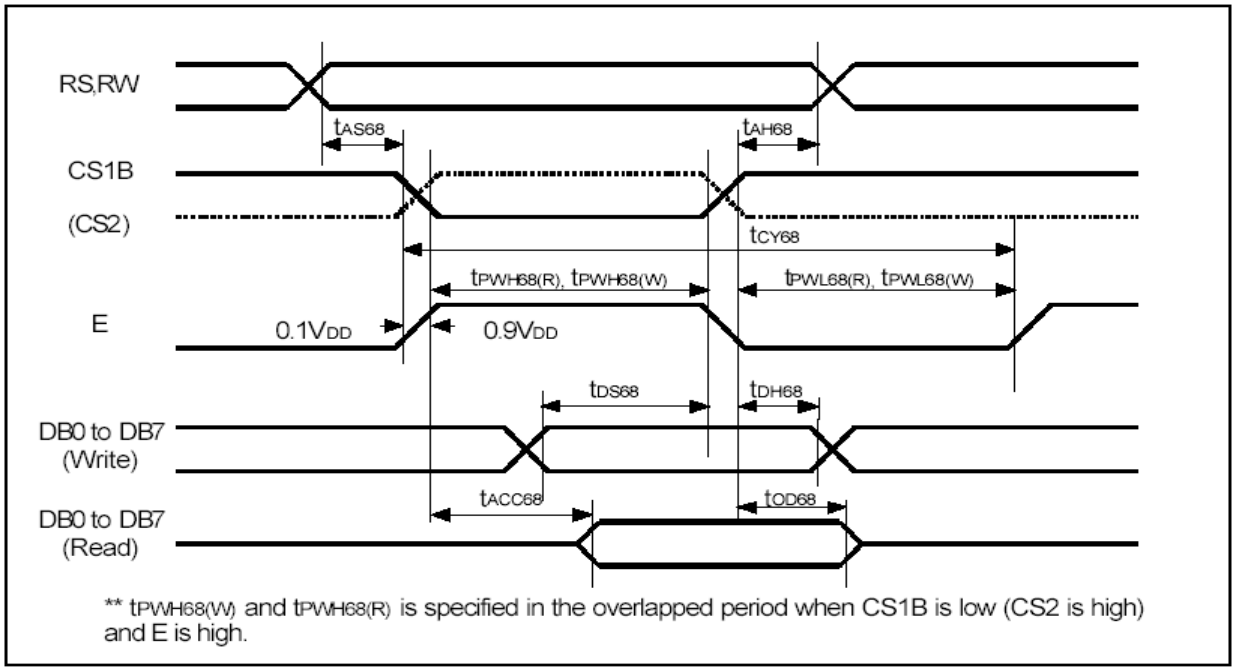
DC characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}	Select by product code	2.4	-	3.6	V	VDD *1
				2.4	-	5.5		
Operating voltage (2)		V0		4.5	-	15.0	V	V0 *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{DD} = 3.0V V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	fOSC	V_{DD} = 3.0V Ta = 25°C Duty ratio = 1/65	32.7	43.6	54.5	kHz	CL *8
	External	fCL		4.09	5.45	6.81		
Voltage converter input voltage		VCI	× 2	2.4	-	5.5	V	VCI
			× 3	2.4	-	5.0		
			× 4	2.4	-	3.75		
			× 5	2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		6.0	-	16.0	V	VOUT
Voltage follower operating voltage		V0		4.5	-	15.0	V	V0 *9
Reference voltage		V_{REF}	V_{DD}= 3.0V Ta = 25°C -0.05%/°C	2.04	2.1	2.16	V	*10

AC characteristics

Read / Write Characteristics (6800-series Microprocessor)



** $t_{PWH68(W)}$ and $t_{PWH68(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and E is high.

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

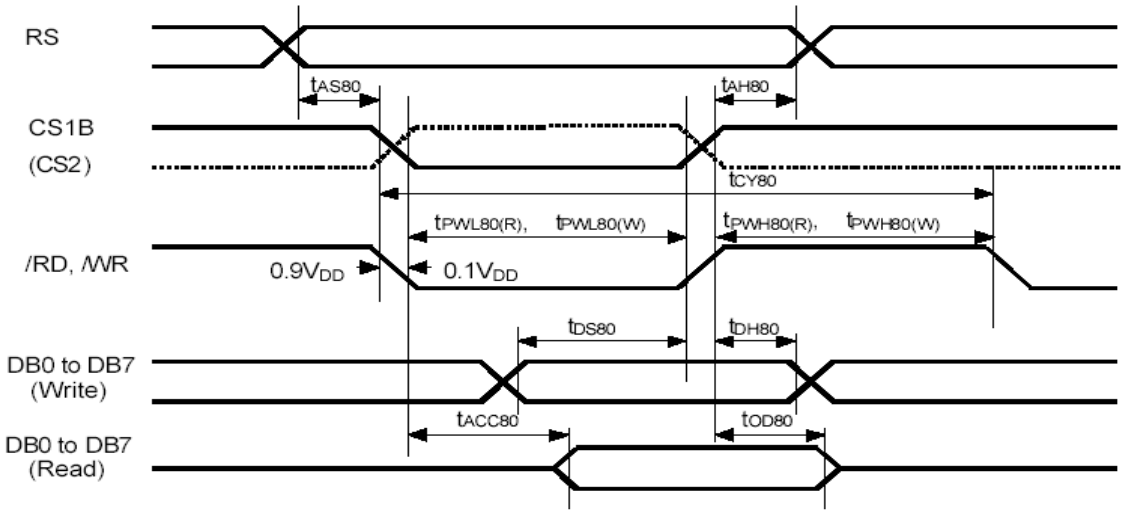
Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	tAS68 tAH68	0 0	-	-	ns	
System cycle time		E	tCY68	300	-	-	ns	
Enable Pulse High Width	Read	E	tPWH68 (R)	120			ns	
	Write		tPWH68 (W)	60				
Enable Pulse Low Width	Read	E	tPWL68 (R)	60			ns	
	Write		tPWL68 (W)	60				
Data setup time Data hold time		DB7 To DB0	tDS68 tDH68	40 15	-	-	ns	
Access time Output disable time			tACC68 tOD68	- 10	-	140 100	ns	CL = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	tAS68 tAH68	0 0	-	-	ns	
System cycle time		E	tCY68	166	-	-	ns	
Enable Pulse High Width	Read	E	tPWH68 (R)	70			ns	
	Write		tPWH68 (W)	30				
Enable Pulse Low Width	Read	E	tPWL68 (R)	30			ns	
	Write		tPWL68 (W)	30				
Data setup time Data hold time		DB7 To DB0	tDS68 tDH68	30 10	-	-	ns	
Access time Output disable time			tACC68 tOD68	- 10	-	70 50	ns	CL = 100 pF

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less. Or (tr + tf) < (t_{CY68} – $t_{PWL68 (W)}$ – $t_{PWH68 (W)}$) for write, (tr + tf) < (t_{CY68} – $t_{PWL68 (R)}$ – $t_{PWH68 (R)}$) for read.

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	tAS80 tAH80	0 0	-	-	ns	
System cycle time		/WR, /RD	tCY80	300	-	-	ns	
Enable Pulse Low width	Read	/RD	tPWL80 (R)	120	-	-	ns	
	Write	/WR	tPWL80 (W)	60	-	-	ns	
Enable Pulse High width	Read	/RD	tPWH80 (R)	60	-	-	ns	
	Write	/WR	tPWH80 (W)	60	-	-	ns	
Data setup time Data hold time		DB7 To DB0	tDS80 tDH80	40 15	-	-	ns	
Read access time Output disable time			tACC80 tOD80	- 10	-	140 100	ns	CL = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	tAS80 tAH80	0 0	-	-	ns	
System cycle time		/WR, /RD	tCY80	166	-	-	ns	
Enable Pulse Low width	Read	/RD	tPWL80 (R)	70	-	-	ns	
	Write	/WR	tPWL80 (W)	30	-	-	ns	
Enable Pulse High width	Read	/RD	tPWH80 (R)	30	-	-	ns	
	Write	/WR	tPWH80 (W)	30	-	-	ns	
Data setup time Data hold time		DB7 To DB0	tDS80 tDH80	30 10	-	-	ns	
Read access time Output disable time			tACC80 tOD80	- 5	-	70 50	ns	CL = 100 pF

Note: The input signal rising time and falling time (tr, tf) is specified at 15ns or less.
Or (tr + tf) < (t_{CY80} – $t_{PWL80 (W)}$ – $t_{PWH80 (W)}$) for write, (tr + tf) < (t_{CY80} – $t_{PWL80 (R)}$ – $t_{PWH80 (R)}$) for read.

Command Set

1. Display On/Off

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	-

D0=1 Display On

D0=0 Display Off

2. Set Display Start Line

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
.	.	.	.	.
0	1	1	1	7
1	0	0	0	8

4.Set Column Address

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	Y7	Y6	Y5	Y4
0	1	0	0	0	0	0	Y3	Y2	Y1	Y0

Y4-Y7 :Higter bits

Y0-Y3 :Lower bits

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

4. Read Status

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status				0	0	0	0

5. Write Display Data

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

6. Read Display Data

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

7. ADC Select

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0

8. Normal/Reverse Display

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D=1 Reverse Display
D=0 Normal Display

9. Entire Display On/Off

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D=0 Normal Display D=1 Reverse Display

10. Set LCD Bias

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

When D=0 Bias=1/9
D=1 Bias=1/7

11. Read-Modify-Write

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

12. End

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

13. Reset

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

15.**Command Output Mode Select**

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

16.**Set Power Control**

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0=1 Follower Circuit Is Turn On

A1=1 Regulator Circuit Is Turn On

A2=1 Booster Circuit Is Turn On

17. **V0 Voltage Regulator Internal Resistor Ratio Set**

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	（1+Rb/Ra）Ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

18.**The Electronic Volume Mode Set**

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

19. Electronic Volume Register Set

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage Parameter	V0	Contrast
0	0	0	0	0	0	0	Minimun	Low
0	0	0	0	0	1	1	.	.
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	32（Default）	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	62	.	.
1	1	1	1	1	1	63	Maximun	High

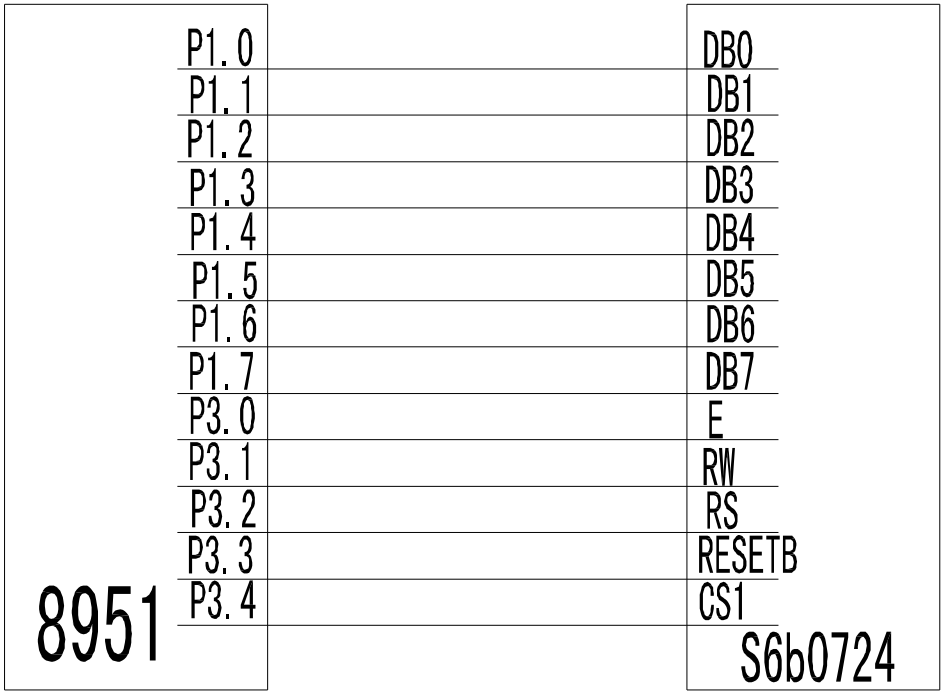
20.**Static Indicator On/Off**

RS	E	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

When D=0: Static Indicator Off D=1:Static Indicator On

Application Example

Application Circuit



Company Profile

XIAMEN OCULAR LCD DEVIDES CO.,LTD. Was formed in 1992. Our company is a joint-venture specializing in manufacturing all kinds of Liquid Crystal Displays. We design and massproduce Touch Panel,LED,COG, the digital segment, dot matrix LCD panels, and modules in TN,HTN and STN types using the advanced and whole facilities and soft-ware technology.

Most of our products are customer_mode. Xiamen Ocular's LCDs now have a good sale not only in domextic China,but also in America,Europe and East_south Aisa.These LCDs were widely used in the display of instruments,clocks,telecommunication equipments,calcuators,air conditioner controllers and AV systems.

Based upon the reliable high quality, reasonable price and quick delivery, Xiamen Ocular will sever all customers wholeheartedly.

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