SPECIFICATION

120*32 Dot Matrix LCD Module

GDSC12032M-01

(COG)

XIAMEN OCULAR LCD DEVIDES CO.,LTD.

GENERAL SPECIFICATION

Interface With **Paraller** MPU

Display Dot Matrix :**120*32**

Display Mode:Positive/Transflective/STN Type

Viewing Angle :**6:00** Clock

Display Duty:**1/32** Driving Bias:**1/6** Driving Voltage:**9.5V**

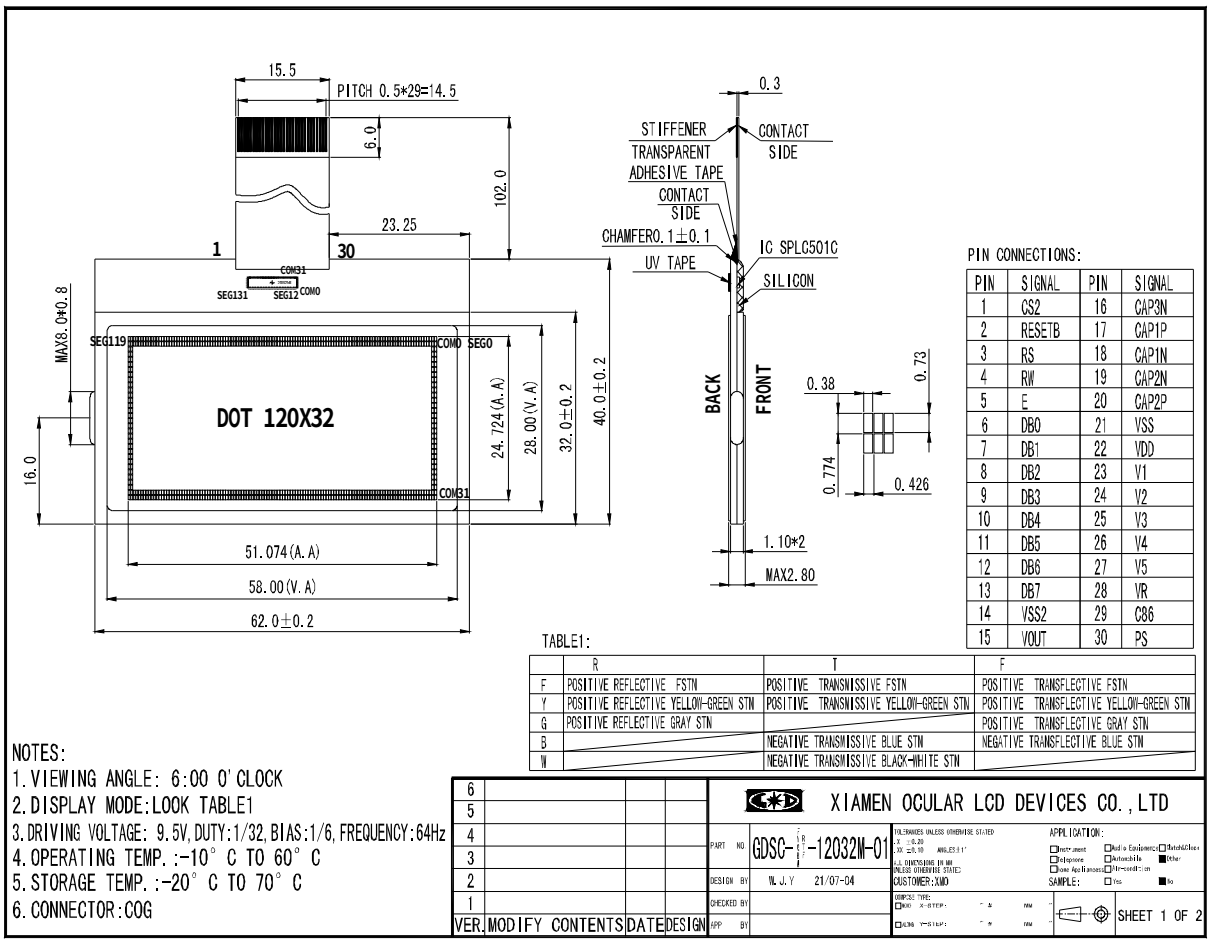
Mechanical Characteristics(Unit:mm)

Extenal Dimension:**62.0*40.0*2.8**

View Area:**51.074*24.724**

Dots Size:**0.38*0.73**

External Dimension



PIN CONNECTIONS:

PIN	SIGNAL	PIN	SIGNAL
1	CS2	16	CAP3N
2	RESETB	17	CAP1P
3	RS	18	CAP1N
4	RW	19	CAP2N
5	E	20	CAP2P
6	DB0	21	VSS
7	DB1	22	VDD
8	DB2	23	V1
9	DB3	24	V2
10	DB4	25	V3
11	DB5	26	V4
12	DB6	27	V5
13	DB7	28	VR
14	VSS2	29	C86
15	VOUT	30	PS

TABLE1:

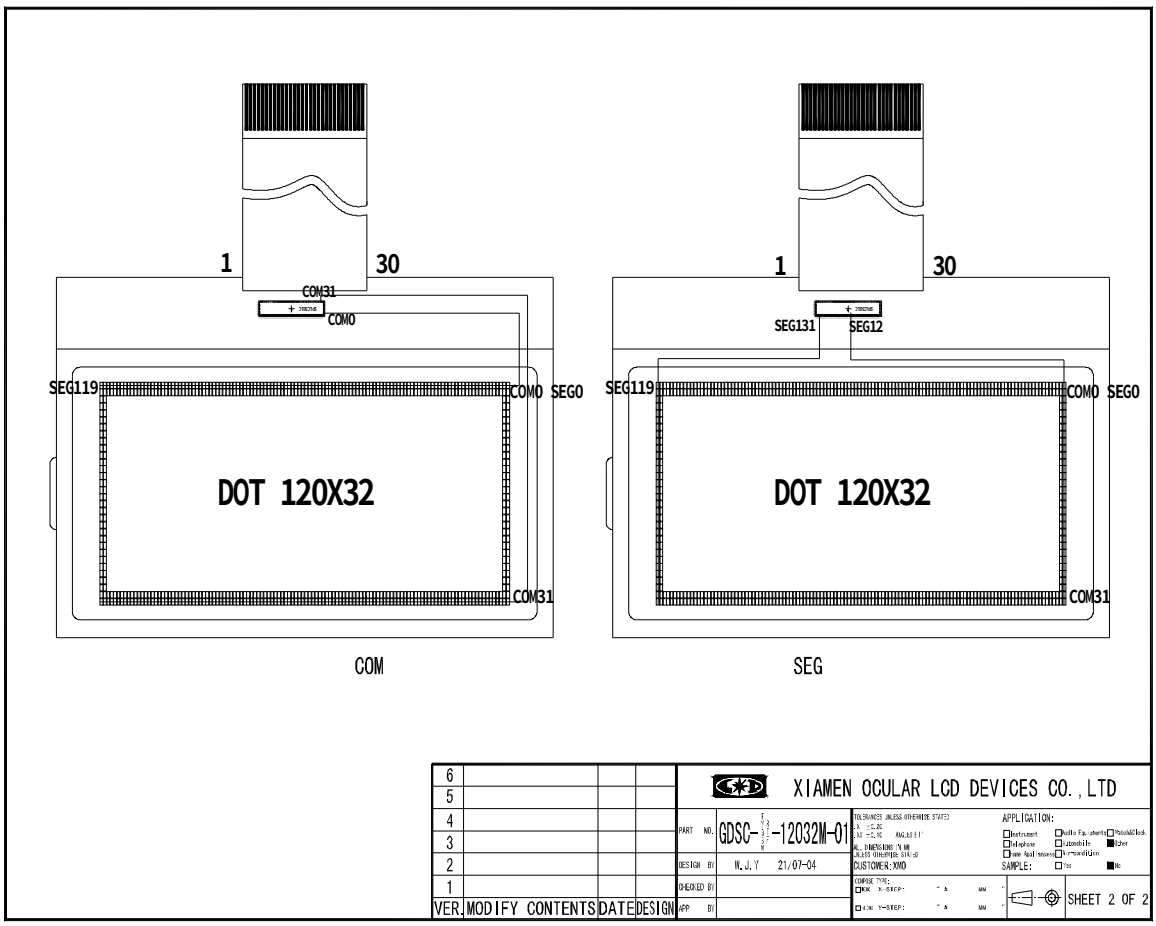
	R	T	F
F	POSITIVE REFLECTIVE FSTN	POSITIVE TRANSMISSIVE FSTN	POSITIVE TRANSFLECTIVE FSTN
Y	POSITIVE REFLECTIVE YELLOW-GREEN STN	POSITIVE TRANSMISSIVE YELLOW-GREEN STN	POSITIVE TRANSFLECTIVE YELLOW-GREEN STN
G	POSITIVE REFLECTIVE GRAY STN		POSITIVE TRANSFLECTIVE GRAY STN
B		NEGATIVE TRANSMISSIVE BLUE STN	NEGATIVE TRANSFLECTIVE BLUE STN
W		NEGATIVE TRANSMISSIVE BLACK-WHITE STN	

NOTES:
1. VIEWING ANGLE: 6:00 O'CLOCK
2. DISPLAY MODE:LOOK TABLE1
3. DRIVING VOLTAGE: 9.5V, DUTY:1/32, BIAS:1/6, FREQUENCY:64Hz
4. OPERATING TEMP.:-10° C TO 60° C
5. STORAGE TEMP.:-20° C TO 70° C
6. CONNECTOR:COG

VER.	MODIFY CONTENTS	DATE	DESIGN
6			
5			
4			
3			
2			
1			

XIAMEN OCULAR LCD DEVICES CO., LTD

PART NO: GDSC-12032M-01
DESIGN BY: WL.J.Y 21/07-04
CHECKED BY:
APP BY:
CUSTOMER:XMD
APPLICATION:
SAMPLE:
SHEET 1 OF 2



VER.	MODIFY CONTENTS	DATE	DESIGN
6			
5			
4			
3			
2			
1			

XIAMEN OCULAR LCD DEVICES CO., LTD

PART NO. GDSC-[illegible]-12032M-01

DESIGN BY W.J.Y 21/07-04

CHECKED BY

APP BY

CUSTOMER: XMD

APPLICATION:

SAMPLE:

SHEET 2 OF 2

Absolute Maximun Ratings

(Unless otherwise noted, VSS = 0V)

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		VDD	-0.3 to + 7.0	V
Power supply voltage (2) (VDD standard)	With Triple step-up	VSS2	-7.0 to +0.3	V
	With Quad step-up		-4.0 to +0.3	
			-3.0 to +0.3	
Power supply voltage (3) (VDD standard)		V_5, V_{OUT}	-12.0 to +0.3	V
Power supply voltage (4) (VDD standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	-0.3 to VDD +0.3	V
Output voltage		V_O	-0.3 to VDD +0.3	V
Operating temperature		T_{OPR}	-40 to +85	℃
Storage temperature	Bare chip	T_{STR}	-55 to +125	℃

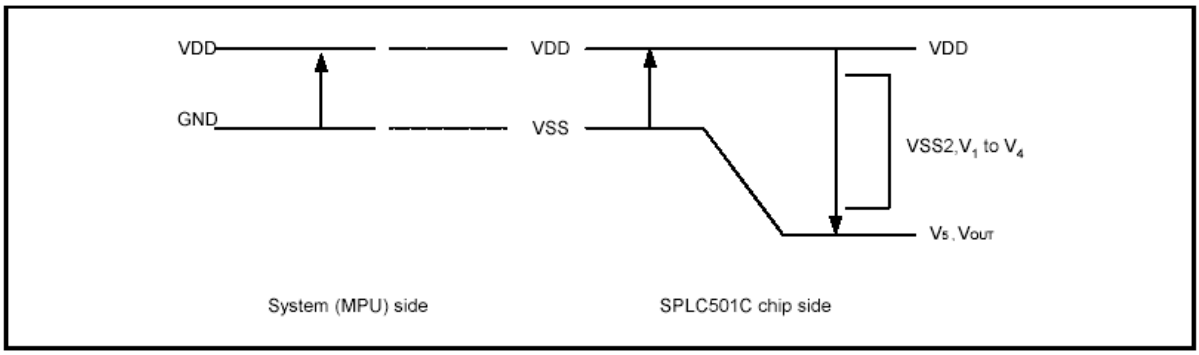


Figure 25

Notes and Cautions:

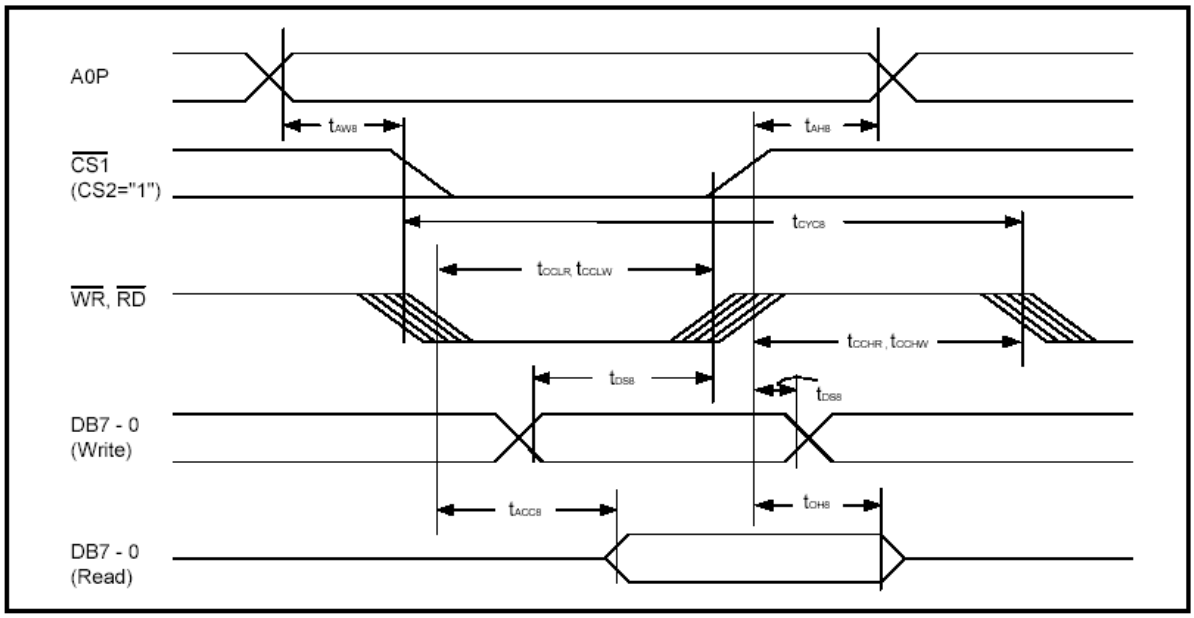
1. The VSS2, V_1 to V_5 and VOUT are relative to the VDD = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that VDD≧V_1≧V_2≧V_3≧V_4≧V_5.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

Electrical Characteristics

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage For logic	Vdd-Vss	-	**2.4**	-	**5.5**	V
Supply Current For logic	Idd	-	-	-	1000	uA
Driving Current For LCD	Iee		-	-	80	uA
Driving Voltage For LCD	V0-Vss		-	-	-	V
Input Voltage H level	Vih		0.7Vdd	-	Vdd	V
Input Voltage L level	Vil		Vss	-	0.3Vdd	V

Timing characteristics

System bus read/write characteristics 1 (8080 Series MPU)



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		166	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	-	ns
Data setup time	DB7 - 0	t_{DS8}		30	-	ns
Address hold time		t_{DH8}		10	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	70	ns
Output disable time		t_{OH8}		5.0	50	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		300	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	-	ns
Data setup time	DB7 - 0	t_{DS8}		40	-	ns
Address hold time		t_{DH8}		15	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	140	ns
Output disable time		t_{OH8}		10	100	ns

(VDD = 2.4V to 2.7V, T_A = 25℃)

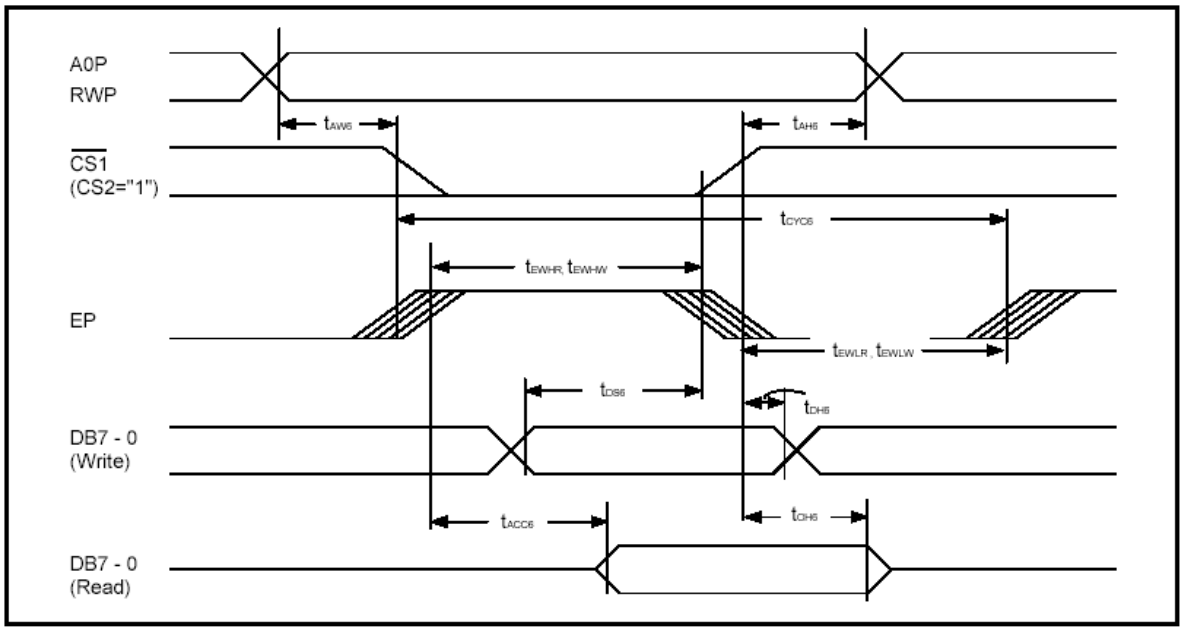
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		1000	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	-	ns
Data setup time	DB7 - 0	t_{DS8}		80	-	ns
Address hold time		t_{DH8}		30	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	280	ns
Output disable time		t_{OH8}		10	200	ns

Note1: The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being 'L' (CS2 = 'H') and $\overline{WR}$ and $\overline{RD}$ being at the 'L' level.

System bus read/write characteristics 2 (6800 Series MPU)



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		166	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	30	-	ns
Data hold time			t_{DH6}		10	-	ns
Access time			t_{ACC6}		-	70	ns
Output disable time			t_{OH6}		10	50	ns
Enable H pulse time	Read	EP	t_{EWHR}		70	-	ns
	Write		t_{EWHW}		30	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		30	-	ns
	Write		t_{EWLW}		30	-	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		300	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	40	-	ns
Data hold time			t_{DH6}		15	-	ns
Access time			t_{ACC6}		-	140	ns
Output disable time			t_{OH6}		10	100	ns
Enable H pulse time	Read	EP	t_{EWHR}		120	-	ns
	Write		t_{EWHW}		60	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		60	-	ns
	Write		t_{EWLW}		60	-	ns

(VDD = 2.4V to 2.7V, T_A = 25℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		1000	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100pF	80	-	ns
Data hold time			t_{DH6}		30	-	ns
Access time			t_{ACC6}		-	280	ns
Output disable time			t_{OH6}		10	120	ns
Enable H pulse time	Read	EP	t_{EWHR}		240	-	ns
	Write		t_{EWHW}		120	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		120	-	ns
	Write		t_{EWLW}		120	-	ns

Note1: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being 'L' (CS2 = 'H') and EP.

IC Specification

See The Reference of SUNPLUS Data Book----SPLC501C

PIN assignment

Pin	Symbol	Function
1	**CS2**	This is the chip select signal .When CS1= "L" and CS2= "H",then the chip select becomes active,and data/command I/O is enabled
2	**RESETB**	When RESETB is set to "L" ,the setting are initialized The RESETB operation is performed by the RESETB signal level
3	**RS**	Select register. 0:Instruction register (for write) Busy flag &address counter(for read) 1:Data register(for write and read).
4	**RW**	Read/write select signal.
5	**E**	Operation (data read/write) enable signal.
6	**DB0**	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then DB7 serves as the serial data input terminal and DB6 serves as the serial clock input terminal.At this time,DB0-DB5 are set to high impedence. When the chip select is inactive,DB0 to DB7 are set to high impedance.
7	**DB1**	
8	**DB2**	
9	**DB3**	
10	**DB4**	
11	**DB5**	
12	**DB6**	
13	**DB7**	
14	**VSS2**	A reference power supply for the step-up voltage circuit for the liquid crystal drive
15	**VOUT**	DC/DC voltage converter output
16	**CAP3-**	Capacitor3- for internal DC/DC voltage converter
17	**CAP1+**	Capacitor1+ for internal DC/DC voltage converter
18	**CAP1-**	Capacitor1- for internal DC/DC voltage converter
19	**CAP2-**	Capacitor2- for internal DC/DC voltage converter
20	**CAP2+**	Capacitor2+ for internal DC/DC voltage converter
21	**VSS**	Ground.
22	**VDD**	Power supply for logic
23	**V1**	LCD driver supply voltages.The voltage determined by LCD cell is impedangce-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship:
24	**V2**	
25	**V3**	
26	**V4**	

<table>
<tr><td>27</td><td>V5</td><td>V0>V1>V2>V3>V4>VSS
When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
<table>
<tr><td>LCD BIAS</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/5BIAS</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 BIAS</td><td>5/6V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 BIAS</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 BIAS</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 BIAS</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>28</td><td>VR</td><td>Voltage adjustment pad.Applies voltage betweem V5 and VSS using a resistive divider</td></tr>
<tr><td>29</td><td>C86</td><td>C86=“H” :6800 series MPU interface
C86=“L” :8080 series MPU interface</td></tr>
<tr><td>30</td><td>PS</td><td>P/S=“H” :Parallel data input
P/S=“L” :serial data input</td></tr>
</table>

Instruction Table

Command	Command Code												Function
	A0P	$\overline{RD}$	$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1). Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1		LCD display ON/OFF 0: OFF, 1: ON
2). Display start line set	0	1	0	0	1	Display start address							Sets the display RAM display start line address
3). Page address set	0	1	0	1	0	1	1	Page address					Sets the display RAM page address
4). Column address set upper bit	0	1	0	0	0	0	1	Most significant column address					Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address					Set the least significant 4 bits of the display RAM column address.
5). Status read	0	0	1	Status				0	0	0	0		Reads the status data
6). Display data write	1	1	0	Write data									Writes to the display RAM
7). Display data read	1	0	1	Read data									Reads from the display RAM
8). ADC select	0	1	0	1	0	1	0	0	0	0	0 1		Sets the display RAM address SEG output correspondence 0: normal, 1:reverse
9). Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1		Sets the LCD display normal/ reverse 0: normal, 1:reverse
10). Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1		Display all points 0: normal display 1: all points ON
11). LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1		Sets the LCD driver voltage bias ratio SPLC501C.....0:1/9, 1:1/7
12). Read/modify/write	0	1	0	1	1	1	0	0	0	0	0		Column address increment At write: +1 At read: 0
13). End	0	1	0	1	1	1	0	1	1	1	0		Clear read/modify/write
14). Reset	0	1	0	1	1	1	0	0	0	1	0		Internal reset
15). Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*		Select COM output scan direction 0: normal direction, 1: reverse direction
16). Power control set	0	1	0	0	0	1	0	1	Operating mode				Select internal power supply operating mode
17). V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio				Select internal resistor ratio (Rb/Ra) mode
18). Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1		Set the V_5 output voltage electronic volume register
Electronic volume register set	0	1	0	*	*	Electronic volume value							

Command	Command Code										Function
	A0P	$\overline{RD}$	$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
19). Static indicator				1	0	1	0	1	1	0	0	0: OFF, 1: ON
ON/OFF											1	
Static indicator				*	*	*	*	*	*	Mode		Set the flashing mode
Register set												
20). Page Blink	0	1	0	1	1	0	1	0	1	0	1	
Page selection	0	1	0	P7	P6	P5	P4	P3	P2	P1	P0	P7 - 0: 1 - blinking page 0 - no blinking, normal display
21). Driving Mode Set	0	1	0	1	1	0	1	0	0	1	0	Set the driving mode register
Mode selection	0	1	0	D1	D0	0	0	0	0	0	0	Driving capability (D1, D0): (1,1)>(0,0)>(0,1)>(1,0)
22). Power saver												Display OFF and display all points ON compound command
23). NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
24). Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command
				1	1	0	1	0	1	0	0	

Instruction Description

1. Display On/Off

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	1	1	1	**-**

D0=1 Display On

D0=0 Display Off

2. Set Display Start Line

A0	RD	WR	D7	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

ST5	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

A0	RD	WR	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	1	**P3**	**P2**	**P1**	**P0**

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
.	.	.	.	.
0	1	1	1	7
1	0	0	0	8

4.Set Column Address

A0	RD	WR	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	0	0	**Y7**	**Y6**	**Y5**	**Y4**
0	1	0	0	0	0	0	**Y3**	**Y2**	**Y1**	**Y0**

Y4-Y7 :Higter Bits

Y0-Y3 :Lower Bits

Y7	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**	**Column Address**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
0	1	0	1	1	1	1	0	94
0	1	0	1	1	1	1	1	95

5. Read Status

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status				0	0	0	0

6. Write Display Data

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7. Read Display Data

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8. ADC Select

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	0	0	**-**

D0=**1** **Display Reverse**

D0=**0** **Display Normal**

9. Normal/Reverse Display

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	1	1	**D**

When **D**=1 Reverse Display

D=0 Normal Display

10. Entire Display On/Off

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When **D**=0 Nornal Display **D**=1 Reverse Display

11. Set LCD Bias

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	0	0	1	**D**

When **D**=0 Bias=1/9

D=1 Bias=1/7

12. Read-Modify-Write

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

13. End

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

14. Reset

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

15.**Command Output Mode Select**

A0	RD	WR	D7	D6	D5	D4	**D3**	D2	D1	D0
0	1	0	1	1	0	0	**D**	*	*	*

16.Set Power Control

A0	RD	WR	D7	D6	D5	D4	D3	**D2**	**D1**	**D0**
0	1	0	0	0	1	0	1	**A2**	**A1**	**A0**

When **A0**=1 Follower Circuit Is Turn on

A1=1 Regulator Circuit Is Turn on

A2=1 Booster Circuit Is Turn on

17. V5 Voltage Regulator Internal Resistor Ratio Set

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

18.The Electronic Volume Mode Set

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

19. Electronic Volume Register Set

A0	RD	WR	D7	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	0	**SV5**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

20.Static Indicator On/Off

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	**D0**
0	1	0	1	0	1	0	1	1	0	**D**

When **D**=0: Static Indicator Off **D**=1:Static Indicator On

21. Page Blinking

The Page Blinking Mode Set

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	1

Page Blinking Register Set

A0	RD	WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BlinkingPage
0	1	0	1	0	0	0	0	0	0	0	Page7 Blink

0	1	0	0	1	0	0	0	0	0	0	Page6 Blink
0	1	0	0	0	1	0	0	0	0	0	Page5 Blink
0	1	0	.	.	.	.	.	.	.	.	.
0	1	0	0	0	0	0	0	0	0	1	Page0 Blink

22. Set Driving Mode Set

The Driving Mode Set

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	0

Mode Selection Register Set

A0	RD	WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Driving Selection
0	1	0	1	1	0	0	0	0	0	0	Mode1
0	1	0	0	0	0	0	0	0	0	0	Mode2
0	1	0	0	0	1	0	0	0	0	0	Mode3
0	1	0	1	0	0	0	0	0	0	1	Mode4

23. Nop

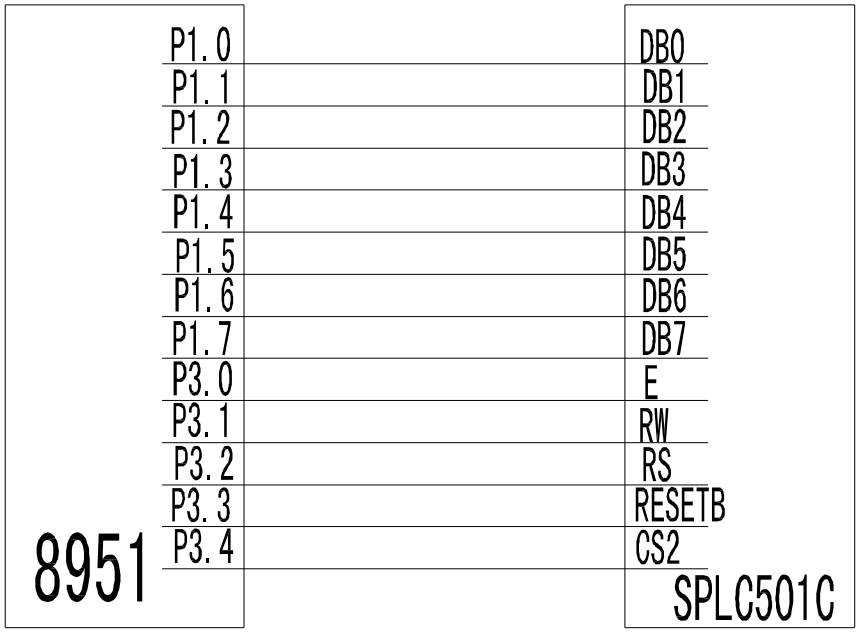
A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

24.Test

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

Application Example

Application Circuit



Program Example

```
E       EQU   P3.0
RW      EQU   P3.1
A0      EQU   P3.2
RES     EQU   P3.3
CS1     EQU   P3.4
COM     EQU   30H
DAT     EQU   31H
        ORG   0000H
        AJMP MAIN
        ORG   0050H
MAIN: CLR   RES
        LCALL DELAY
        SETB  RES
        MOV   COM,#0E2H
        LCALL  PR1
        LCALL  DELAY
        LCALL  DELAY
        MOV   COM,#0A1H
        LCALL  PR1
        MOV   COM,#0AEH
        LCALL  PR1
        MOV  COM,#0C0H
        LCALL PR1
        MOV  COM,#0A3H
        LCALL  PR1
        MOV  COM,#02FH
        LCALL  PR1
        MOV  COM,#0A6H
        LCALL  PR1
        MOV   COM,#0A4H
        LCALL  PR1
        MOV   COM,#0ACH
        LCALL  PR1
        MOV   COM,#040H
        LCALL  PR1
        MOV   COM,#025H
        LCALL  PR1
        MOV  COM,#081H
        LCALL  PR1
        MOV   COM,#1FH
        LCALL    PR1
```

GDSC-12032M-01

Company Profile

XIAMEN OCULAR LCD DEVIDES CO.,LTD. Was formed in 1992. Our company is a joint-venture specializing in manufacturing all kinds of Liquid Crystal Displays. We design and massproduce Touch Panel,LED,COG, the digital segment, dot matrix LCD panels, and modules in TN,HTN and STN types using the advanced and whole facilities and soft-ware technology.

Most of our products are customer_mode. Xiamen Ocular's LCDs now have a good sale not only in domextic China,but also in America,Europe and East_south Aisa.These LCDs were widely used in the display of instruments,clocks,telecommunication equipments,calcuators,air conditioner controllers and AV systems.

Based upon the reliable high quality, reasonable price and quick delivery, Xiamen Ocular will sever all customers wholeheartedly.

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